1. BF7515CM44-LJTX MCU General Description

1.1. Features

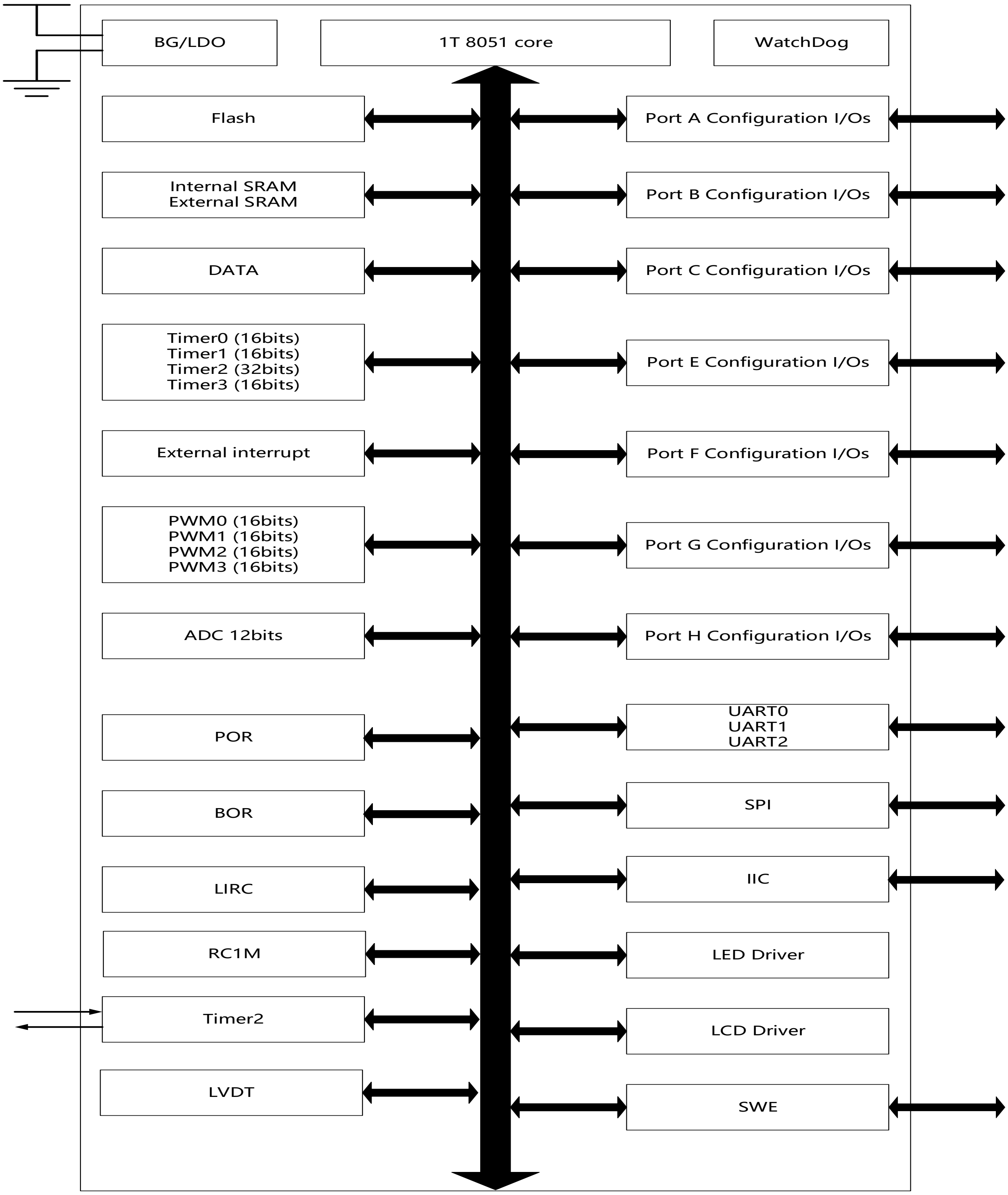
- **Core: 1T 8051**
  - Operating frequency: 12MHz, 8MHz, 4MHz, 1MHz
  - Clock error: ±1% @-20℃~65℃, 5V
    ±3% @-40℃ ~105℃, 5V
- **Memory (FLASH)**
  - CODE: 63K Bytes
  - DATA: 1K Bytes +2*512 Bytes
  - SRAM: 256 Bytes(data)+4K Bytes(xdata)
  - Support 2K/4K/8K BOOT function area
- **Clock Source, Reset and Power Management**
  - Internal low-speed clock LIRC: 32kHz,
    Clock error: ±25%@25℃, 5V, ±35% @-40℃ ~105℃, 5V
  - Internal high-speed RC oscillator: 1MHz
  - External crystal oscillator: 32768Hz/4MHz
  - 8 resets, brown-out reset voltage (Bor): 2.3V/2.8V/3.3V/3.7V/4.2V
  - Low voltage detection: 2.7V/3.0V/3.3V/3.6V/3.8V/ 4.0V/4.2V/4.4V
- **IO**
  - Both support built-in pull-up resistor 35k
  - High current sink port (PB0~PB7)
  - Support IO function remapping
  - Support external interrupt function, INT0~3 (rise-edge, falling-edge, double-edge) and INT4(rise-edge, falling-edge) share interrupt source
- **Communication Module**
  - 3*UART Communication Module
  - 1*IIC slave mode, support 100/400kHz
  - 1*SPI, support up to 2MHz communication
- **16-Bit PWM**
  - PWM0 supports 5 channels, the same period and duty cycle, configurable polarity
  - PWM1 supports 5 channels, the same period and duty cycle, configurable polarity
  - PWM2 supports 1 channel output
  - PWM3 supports 1 channel output
- **Operating Voltage: 2.7V ~ 5.5V**
- **Operating Temperature: -40℃ ~ 105℃**
  - Enhanced industrial grade, in line with JESD industrial grade reliability certification standards
- **12-bit High-precision ADC**
  - Up to 42 analog input channels
  - Reference voltage: VCC/2V/4V
- **Interrupt**
  - Two-level interrupt priority selectable
  - ADC, LED, LCD, INT0/1/2/3/4,LVDT,Timer0~3, WDT, UART0/1/2, IIC, PWM0/1, SPI Interrupt
- **Timer**
  - 16-bit Timer0/1/3, 32-bit Timer2
  - Timer2 clock source: LIRC32k, XTAL32768Hz/4MHz
  - Watchdog timer, overflow time 18ms to 2.304s
- **LED Driver**
  - Support 4x5, 5x6, 6x7, 7x8 dot matrix driver
  - LED0~LED7 scan order can be configured
  - Row and column matrix drive: duty cycle 1/8~8/8
  - LED drive matrix: max 8COM x 8SEG
- **LCD Driver**
  - 4 COM x 28 SEG (1/4 duty cycle, 1/3 bias)
  - 5 COM x 27 SEG (1/5 duty cycle, 1/3 bias)
  - 6 COM x 26 SEG (1/6 duty cycle, 1/3 or 1/4 bias)
  - 8 COM x 24 SEG (1/8 duty cycle, 1/4 bias)
- **Low power management**
  - Idle mode 0 and Idle mode 1
  - Idle mode 1, power consumption 12μA @5V
- **Two-wire programming and single-wire debugging**
- **Package**
  - LQFP44

1.2. Overview

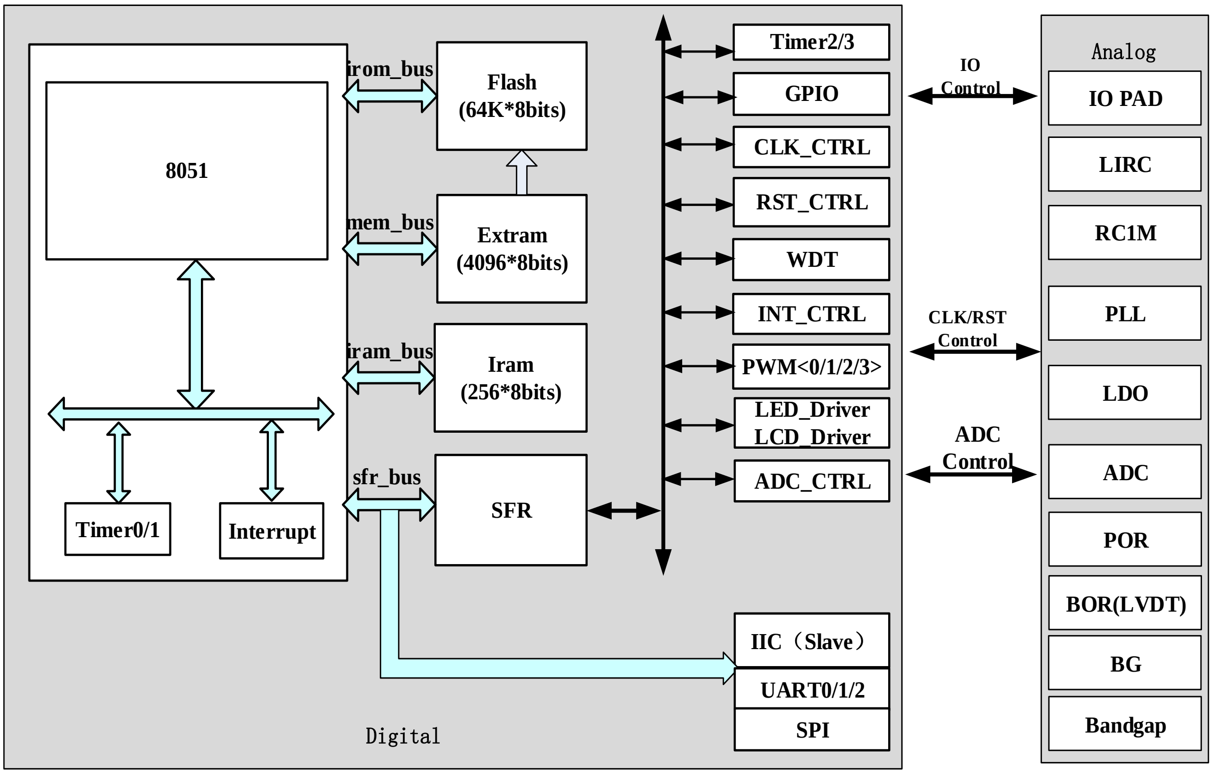
The BF7515CM44-LJTX uses the high speed 8051 core with 1T instruction cycle, based on standard 8051 instruction pipeline structure. Compared to the standard 8051 (12T) instruction cycle, it has the quicker running speed, compatibility standard 8051 instruction.

The BF7515CM44-LJTX includes external watchdog, LED serial dot matrix driver, LCD display driver, IIC, UART, SPI, low voltage detection, power-down reset, 4 independent 16bit PWM modules, Timer0, Timer1, Timer2, Timer3, 12bit successive approximation ADC, low power management, etc.

1.3. System Architecture

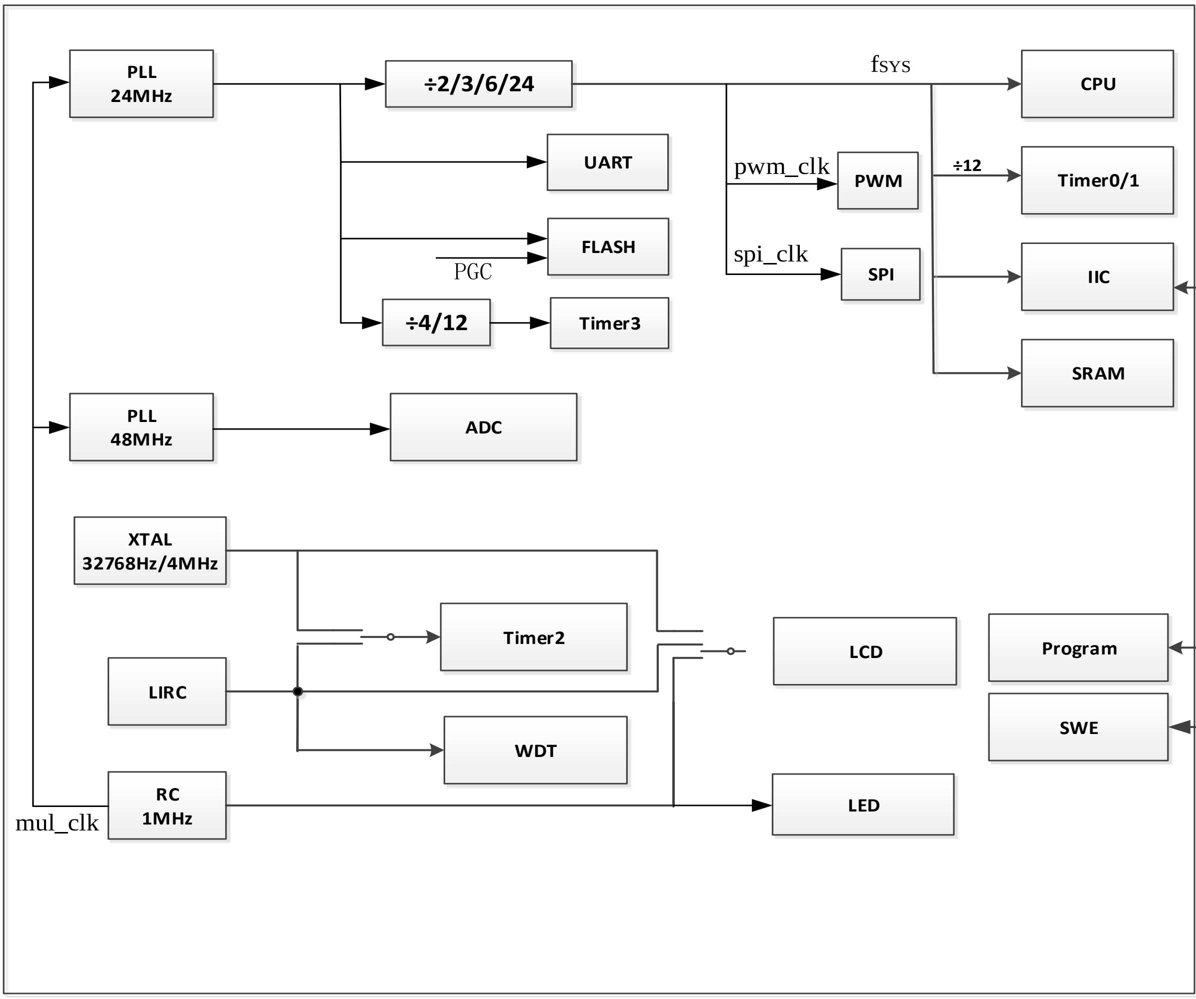


System architecture



System bus frame diagram

1.4. Clock Diagram



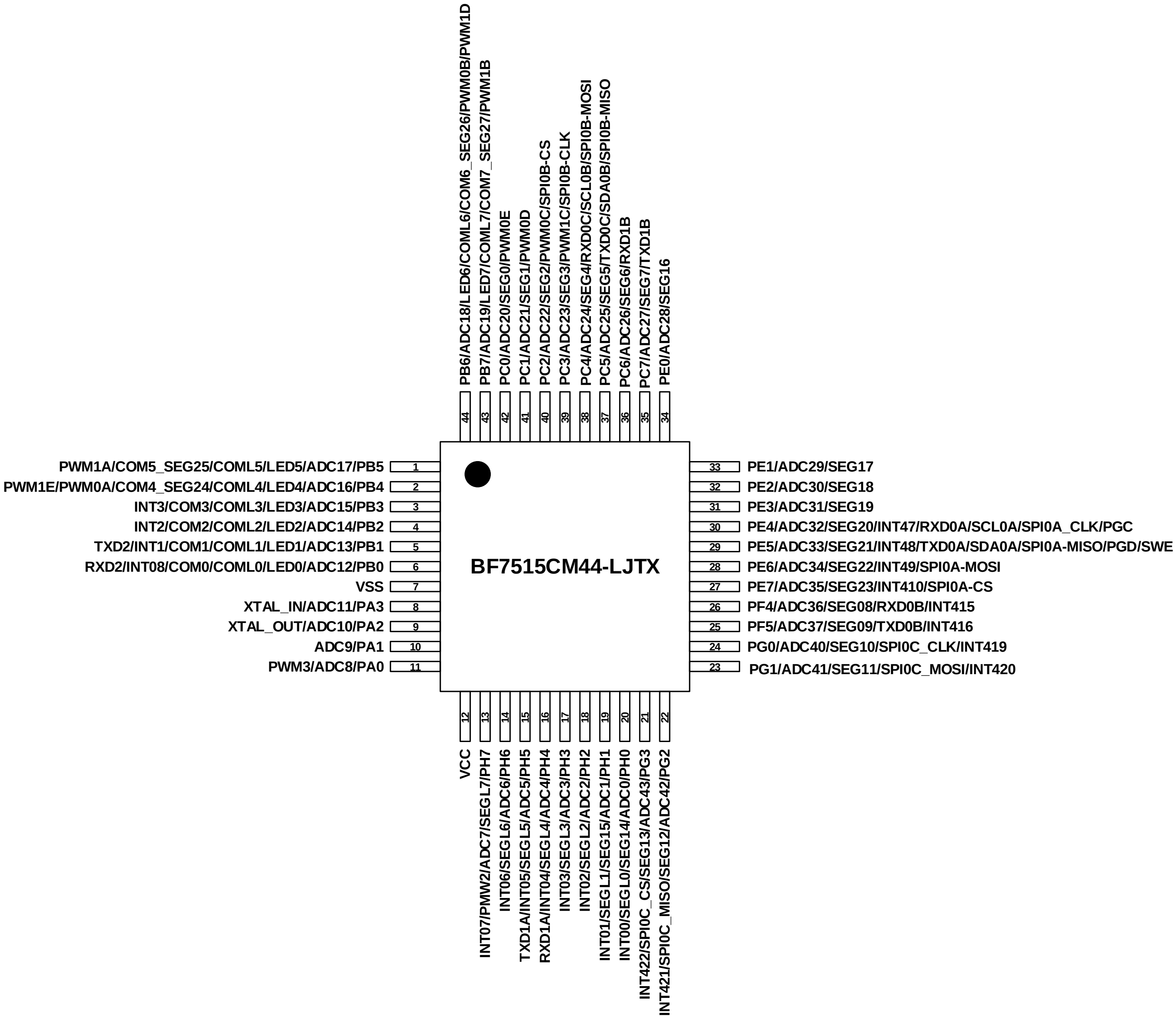
Clock block diagram

1.5. Selection List

Type		BF7515CM44-LJTX
Operation voltage (V)		2.7~5.5
Operating frequency (Hz)		12M
Core		1T 8051
Memory (Bytes)	CODE	63/61/59/55K
	BOOT	0/2/4/8K
	DATA	1K +2*512
	SRAM	256 +4K
Timer	WDT	1
	Timer0*16bit	1
	Timer1*16bit	1
	Timer2*32bit	1
	Timer3*16bit	1
Communication module	IIC	1
	UART	3
	SPI	1
Analog module	ADC*12 bit	42
GPIO		42
COM		8
INT		22
Display module	LED serial	7*8
	LED ranks	8COM*8SEG
	LCD	8COM*24SEG
PWM module	PWM0*16bit	5
	PWM1*16bit	5
	PWM2*16bit	1
	PWM3*16bit	1
Package		LQFP44(10mm*10mm, e=0.8mm)

Selection List

1.6. Pin Assignment



BF7515CM44-LJTX LQFP44 Package pin diagram

1.7. Pin Description

BF7515CM44-LJTX	Function description
1	Default function: GPIO <PB5> Other function: ADC17: ADC channel LED5: LED serial dot matrix COML5: LED matrix COM; Large sink current port COM5_SEG25: COM of LCD can be shared as SEG PWM1A: PWM1A output port
2	Default function: GPIO <PB4> Other function: ADC16: ADC channel LED4: LED serial dot matrix COML4: LED matrix COM; Large sink current port COM4_SEG24: COM of LCD can be shared as SEG PWM0A: PWM0A output port PWM1E: PWM1E output port
3	Default function: GPIO <PB3> Other function: ADC15: ADC channel LED3: LED serial dot matrix COML3: LED matrix COM; Large sink current port COM3: COM of LCD INT3: External Interrupt
4	Default function: GPIO <PB2> Other function: ADC14: ADC channel LED2: LED serial dot matrix COML2: LED matrix COM; Large sink current port COM2: COM of LCD INT2: External Interrupt
5	Default function: GPIO <PB1> Other function: ADC13: ADC channel LED1: LED serial dot matrix COML1: LED matrix COM; Large sink current port COM1: COM of LCD INT1: External Interrupt TXD2: Serial port transmission
6	Default function: GPIO <PB0> Other function: ADC12: ADC channel LED0: LED serial dot matrix COML0: LED matrix COM; Large sink current port COM0: COM of LCD INT08: External Interrupt

	RXD2: Serial port receiving
7	Default function: GND <VSS>
8	Default function: GPIO <PA3> Other function: ADC11: ADC channel XTAL_IN: External crystal oscillator input
9	Default function: GPIO <PA2> Other function: ADC10: ADC channel XTAL_OUT: External crystal oscillator output
10	Default function: GPIO <PA1> Other function: ADC9: ADC channel
11	Default function: GPIO <PA0> Other function: ADC8: ADC channel PWM3: PWM3 output port
12	Default function: power supply <VCC>
13	Default function: GPIO <PH7> Other function: SEGL7: SEG of LED column matrix ADC7: ADC channel PWM2: PWM2 output port INT07: External Interrupt
14	Default function: GPIO <PH6> Other function: SEGL6: SEG of LED column matrix ADC6: ADC channel INT06: External Interrupt
15	Default function: GPIO <PH5> Other function: SEGL5: SEG of LED column matrix ADC5: ADC channel INT05: External Interrupt TXD1A: Serial port transmission
16	Default function: GPIO <PH4> Other function: SEGL4: SEG of LED column matrix ADC4: ADC channel INT04: External Interrupt RXD1A: Serial port receiving
17	Default function: GPIO <PH3> Other function: SEGL3: SEG of LED column matrix ADC3: ADC channel INT03: External Interrupt
18	Default function: GPIO <PH2> Other function: SEGL2: SEG of LED column matrix ADC2: ADC channel INT02: External Interrupt

19	Default function: GPIO <PH1> Other function: SEGL1: SEG of LED column matrix ADC1: ADC channel SEG15: SEG of LCD INT01: External Interrupt
20	Default function: GPIO <PH0> Other function: SEGL0: SEG of LED column matrix ADC0: ADC channel SEG14: SEG of LCD INT00: External Interrupt
21	Default function: GPIO <PG3> Other function: ADC43: ADC channel SEG13: SEG of LCD SPI0C_CS: SPI chip select signal INT422: External Interrupt
22	Default function: GPIO <PG2> Other function: ADC42: ADC channel SEG12: SEG of LCD SPI0C_MISO: SPI master data input INT421: External Interrupt
23	Default function: GPIO <PG1> Other function: ADC41: ADC channel SEG11: SEG of LCD SPI0C_MOSI: SPI master data output INT420: External Interrupt
24	Default function: GPIO <PG0> Other function: ADC41: ADC channel SEG10: SEG of LCD SPI0C_CLK: SPI clock INT419: External Interrupt
25	Default function: GPIO <PF5> Other function: ADC37: ADC channel SEG09: SEG of LCD TXD0B: Serial port transmission INT416: External Interrupt
26	Default function: GPIO <PF4> Other function: ADC36: ADC channel SEG08: SEG of LCD RXD0B: Serial port receiving INT415: External Interrupt

27	Default function: GPIO <PE7> Other function: ADC35: ADC channel SEG23: SEG of LCD INT410: External Interrupt SPI0A_CS: SPI chip select signal
28	Default function: GPIO <PE6> Other function: ADC34: ADC channel SEG22: SEG of LCD INT49: External Interrupt SPI0A_MOSI: SPI master data output
29	Default function: GPIO <PE5> Other function: ADC33: ADC channel SEG21: SEG of LCD INT48: External Interrupt TXD0A: Serial port transmission PGD: Programming port PGD SDA0A: Serial data line of IIC SWE: Single-line simulation SPI0A_MISO: SPI master data input
30	Default function: GPIO <PE4> Other function: ADC32: ADC channel SEG20: SEG of LCD INT47: External Interrupt RXD0A: Serial port receiving PGC: Programming port PGC SCL0A: Serial clock line of IIC SPI0A_CLK: SPI clock
31	Default function: GPIO <PE3> Other function: ADC31: ADC channel SEG19: SEG of LCD
32	Default function: GPIO <PE2> Other function: ADC30: ADC channel SEG18: SEG of LCD
33	Default function: GPIO <PE1> Other function: ADC29: ADC channel SEG17: SEG of LCD
34	Default function: GPIO <PE0> Other function: ADC28: ADC channel SEG16: SEG of LCD
35	Default function: GPIO <PC7> Other function: ADC27: ADC channel

	SEG7: SEG of LCD TXD1B: Serial port transmission
36	Default function: GPIO <PC6> Other function: ADC26: ADC channel SEG6: SEG of LCD RXD1B: Serial port receiving
37	Default function: GPIO <PC5> Other function: ADC25: ADC channel SEG5: SEG of LCD TXD0C: Serial port transmission SDA0B: Serial data line of IIC SPI0B_MISO: SPI master data input
38	Default function: GPIO <PC4> Other function: ADC24: ADC channel SEG4: SEG of LCD RXD0C: Serial port receiving SCL0B: Serial clock line of IIC SPI0B_MOSI: SPI master data output
39	Default function: GPIO <PC3> Other function: ADC23: ADC channel SEG3: SEG of LCD PWMXX: PWM output port SPI0B_CLK: SPI clock
40	Default function: GPIO <PC2> Other function: ADC22: ADC channel SEG2: SEG of LCD PWM0C: PWM output port SPI0B_CS: SPI chip select signal
41	Default function: GPIO <PC1> Other function: ADC21: ADC channel SEG1: SEG of LCD PWM0D: PWM output port
42	Default function: GPIO <PC0> Other function: ADC20: ADC channel SEG0: SEG of LCD PWM0E: PWM output port
43	Default function: GPIO <PB7> Other function: ADC19: ADC channel LED7: LED serial dot matrix COML7: COM of LCD can be shared as SEG COM7_SEG27: COM of LCD can be shared as SEG

	PWM1B: PWM output port
44	Default function: GPIO <PB6> Other function: ADC18: ADC channel LED6: LED serial dot matrix COML6: COM of LCD can be shared as SEG COM6_SEG26: COM of LCD can be shared as SEG PWM0B: PWM output port PWM1D: PWM output port

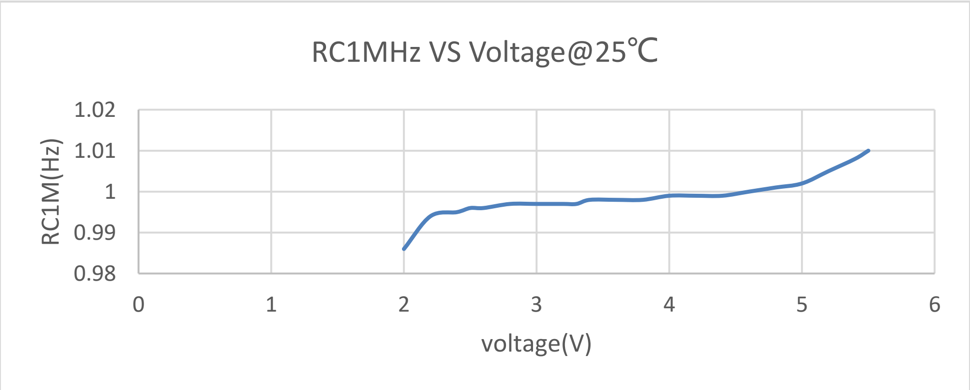
Package pin correspondence diagram

2. Electrical Characteristics

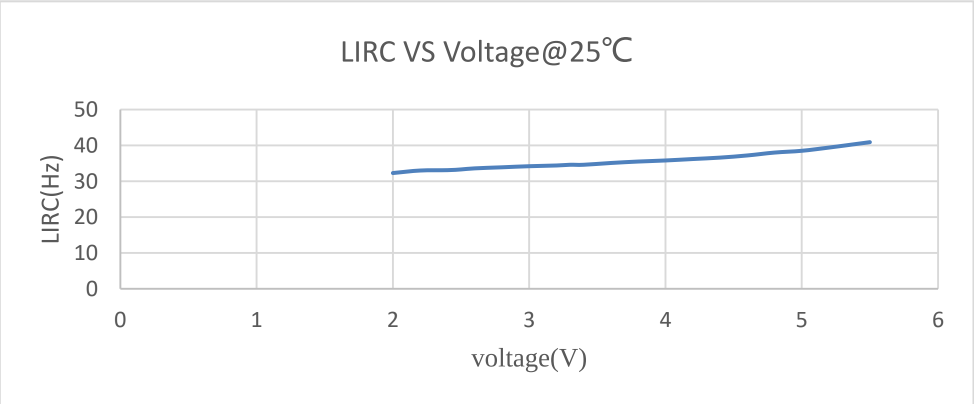
2.1. AC Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
		VCC	Temperature				
f_{RC1M}	Internal high-speed RC oscillator	5V	-20℃~65℃	-1%	1	+1%	MHz
			-40℃ ~105℃	-3%	1	+3%	
		2.7V~5.5V	25℃	-1%	1	+1%	
			-40℃ ~105℃	-3%	1	+3%	
f_{SYS}	System clock	5V	-20℃~65℃	-1%	12/8/4/1	+1%	MHz
			-40℃ ~105℃	-3%	12/8/4/1	+3%	
		2.7V~5.5V	25℃	-1%	12/8/4/1	+1%	
			-40℃ ~105℃	-3%	12/8/4/1	+3%	
f_{LIRC}	Internal low-speed RC oscillator	5V	25℃	-25%	32	+25%	kHz
			-40℃ ~105℃	-35%	32	+35%	
		2.7V~5.5V	25℃	-35%	32	+35%	

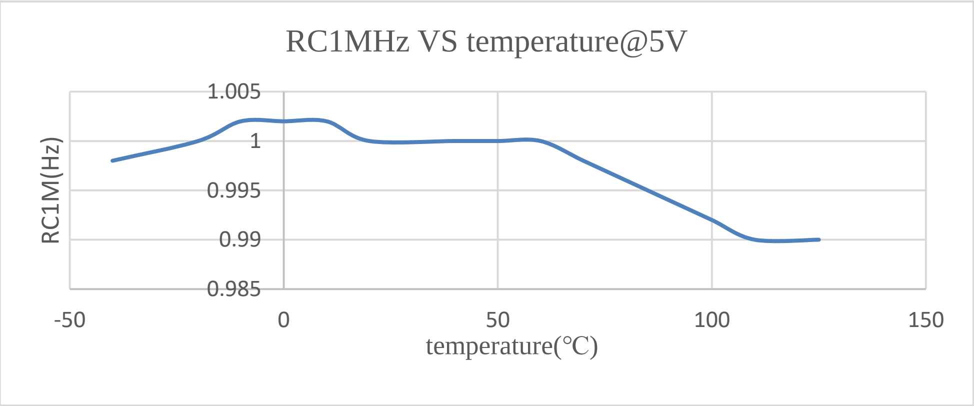
AC characteristic parameter table



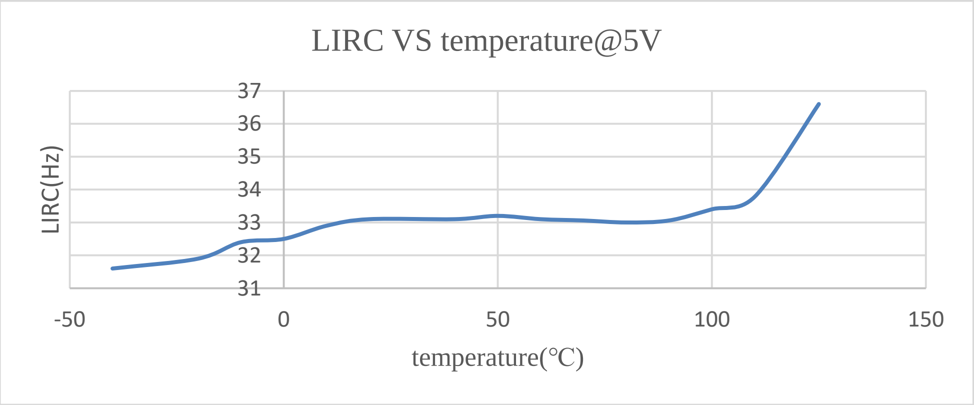
f_{RC1M} voltage curve



f_{LIRC} voltage curve



f_{RC1M} temperature curve



f_{LIRC} temperature curve

2.2. DC Characteristics

Ta=25°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
VCC	Operating Voltage	-	-	2.7	-	5.5	V
I_{OP}	Active mode current	3.3V	f_{RC1M}/ PLL on, f_{SYS} =12MHz, f_{LIRC} on, no load, all peripherals off	-	2.6	3.4	mA
		5V		-	2.7	3.5	
		3.3V	f_{RC1M}/ PLL on, f_{SYS}=8 MHz, f_{LIRC} on, no load, all peripherals off	-	2.3	3.0	
		5V		-	2.4	3.1	
		3.3V	f_{RC1M}/ PLL on, f_{SYS}=4 MHz, f_{LIRC} on, no load, all peripherals off	-	2.0	2.5	
		5V		-	2.0	2.6	
		3.3V	f_{RC1M}/ PLL on, f_{SYS}=1 MHz, f_{LIRC} on, no load, all peripherals off	-	1.6	2.1	
		5V		-	1.7	2.2	
I_{STB0}	idle mode 0 current	3.3V	f_{RC1M}/ PLL on, f_{SYS} off, f_{LIRC} on, all peripherals off	-	1.5	2.1	mA
		5V		-	1.6	2.0	
I_{STB1}	idle mode 1 current	3.3V	f_{RC1M}/ PLL/ f_{SYS} off, f_{LIRC} on, all peripherals off	-	14	18.2	μA
		5V		-	12	15.6	
I_{STB2}	Average current for intermittent wake-up from idle mode 1	3.3V	WDT_CTRL=7, WDT interrupt 2s wake up, 2ms working time, IO output is low, close other functions	-	16.4	21.3	μA
		5V		-	15	19	
		3.3V	Timer2 external crystal oscillator wakes up in 2s, 2ms working time, IO output is low, and other functions are closed	-	16.4	21.3	μA
		5V		-	15	19	
V_{IL}	Input low level	2.7~5.5V	-	-	-	0.3*VCC	V
V_{IH}	Input high level	2.7~5.5V	-	0.7*VCC	-	-	V
V_{INTL}	INT input low level	2.7~5.5V	-	-	-	0.3*VCC	V

V_{INTH}	INT input high level	2.7~5.5V	-	0.7*VCC	-	-	V
V_{OL}	output low voltage	5V	I_{OL}=68mA	-	-	0.1*VCC	V
V_{OH}	output high voltage	5V	I_{OH}=16mA	0.9*VCC	-	-	V
I_{OL}	IO sink current	5V	V_{OL}=0.1VCC	48	68	88	mA
I_{OH}	IO Source current	5V	V_{OH}=0.9VCC	11	16	20	mA
I_{COM}	PB large sink current	5V	V_{OL}=0.1VCC	-	130	-	mA
I_{Leak}	Input leakage current	5V	-	-	1	5	μA
R_{PH}	IO internal pull-up	5V	-	25	35	46	kΩ

The working current of the module is shown in the table below:

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
I_{BOR}	BOR operating current	5V	In idle mode 1, no load, BOR enabled		4. 9	-	μA
I_{LVDT}	LVDT operating current	5V	In idle mode 1, no load, LVDT enabled, voltage selection 3.8V	-	4.8	-	μA
I_{ADC}	ADC operating current	5V	f_{SYS}=12MHz, no load, ADC enable, open a channel, GET_ADC scan, other peripherals off	-	2.1	-	mA
I_{PWM}	PWM operating current	5V	f_{SYS}=12MHz, no load, PWM0 is enabled, other peripherals off	-	0.5	-	mA
I_{ERASE}	Page erase Current	5V	No load, enable NVR3, only NVR3 is erased in while, other peripherals off		2.1	-	mA
I_{PROG}	Programming current	5V	No load, enable NVR3, write only one byte in while, other peripherals off		2.9	-	mA

2.3. ADC Characteristics

Ta=25°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
V_{ADC}	Supply Voltage	-	-	2.7	-	5.5	V
N_R	Accuracy	-	-	-	9	10	Bit
V_{ADCI}	ADC Input voltage	-	-	VSS	-	V_{REF}	V
R_{ADCI}	ADC Input resistance	5V	No RC filtering	1.2	3.2	17.5	kΩ
			RC filtering	10	14.2	31.5	
I_{ADC}	ADC operating current	5V	f_{SYS}=12MHz, enable ADC, open a channel	-	2.1	-	mA
I_{ADCI}	input current	-	-	-	-	1	μA
DNL	Differential nonlinear error	5V	-	-	±4	±6	LSB
INL	Integral nonlinear error	5V	-	-	±4	±6	LSB
t1	ADC sampling time	-	-	0.5	-	-	μs
t_{ADC}	ADC conversion time	-	-	2.875	-	-	μs
RESO	Resolution	-	-	12			Bit
N_{ADC}	Input channel	-	-	-	-	42	Channel

ADC characteristic parameter table

2.4. Limit Parameters

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		VCC	Conditions				
VCC	Supply voltage when working	-	-	VSS+2.7	-	VSS+5.5	V
T_{STG}	Non-working storage temperature	-	-	-40	-	125	℃
Ta	Operating temperature	-	-	-40	-	105	℃
Vin	I/O input voltage	-	-	VSS-0.5	-	VCC+0.5	V
I_{VCC}	Power supply VCC current	-	-	130			mA
I_{VSS}	Ground VSS current	-	-	130			mA
I_{OLA}	IOL total current	-	-	130			mA
I_{OHA}	IOH total current	-	-	-130			mA
ESD(HBM)	Port electrostatic discharge voltage	-	-	-8	-	8	kV

Limit parameters characteristics parameters table

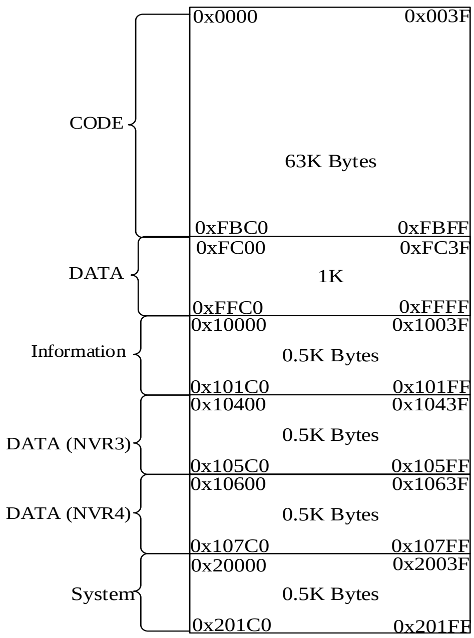
Notes: Exceed the limit parameters may cause damage to the chip, unable to expect the chip work outside the above indicated range. If you work under conditions outside the marked range for a long time, it may affect the reliability of the chip.

3. Memory and SFR

3.1. Memory

FLASH main features:

- CODE area: ICP programming supports block erasing, page erasing and byte writing
- DATA area: page erasing and byte writing
- Program/erase time: CODE area: at least 20000 times@25℃
  DATA area: at least 20000 times@25℃
- Data retention period: 100 years@25℃
  10 years@85℃
- IAP BOOT upgrade function, storage protection, 2K/4K/8K BOOT function area



Flash Storage Architecture

Module	Size (Bytes)	Address	Page
CODE	63K	0x0000~0xFFFF	126
DATA	1K	0xFC00~0xFFFF	1
Information	512	0x10000~0x101FF	1
NVR3	512	0x10400~0x105FF	1
NVR4	512	0x10600~0x107FF	1
System	512	0x20000~0x201FF	1

Address allocation table

3.1.1. Information and System

The main function of the information block is to store configuration words. The configuration word CFG_11 is stored in the system block. There are two ways to read the configuration word of BF7515CMXX-LJTX.

- **Method 1: Read steps**
  1. Turn off the interrupt;
  2. Configure SPROG_CMD = 0x88;
  3. Configure SPROG_ADDR_L, SPROG_ADDR_H, Select the address to be read;
  4. Read SPROG_RDATA data;
  5. Need to continue to read data, jump to step 2 and 3;
  6. After reading SPROG_RDATA data, Configure SPROG_CMD = 0x00;
  7. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00; Restore interrupt settings.
- **Method 2: Read steps**
  1. Turn off the interrupt;
  2. Configure the secondary bus address;
  3. Read data;
  4. Need to continue to read data, skip to step 2 and 3;
  5. Restore interrupt settings.

{SPROG_ADDR_H，SPROG_ADDR_L} The logical address (0x4000+(0~511)) corresponds to the physical address (0x10000~0x101FF)

{SPROG_ADDR_H，SPROG_ADDR_L} The logical address (0x8000+(0~511)) corresponds to the physical address (0x20000~0x201FF)

3.1.2. Unique Identification Code

Steps to read the unique identification code (UID) of the chip:

1. Off the interrupt;
2. Configure SPROG_CMD = 0x88;
3. Configure SPROG_ADDR_L, SPROG_ADDR_H, select the address to be read, 0x41A8~0x41B7 corresponds to product ID1~ID16;
4. Read SPROG_RDATA data;
5. Need to continue to read data, jump to step 2 and 3;
6. After reading SPROG_RDATA data, configure SPROG_CMD = 0x00;
7. corresponds SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00; restore interrupt settings.

3.1.3. Registers

Address	Name	RW	Reset	Description
0xCE	SPROG_ADDR_H	RW	0000_0000b	Address control register
0xCF	SPROG_ADDR_L	RW	0000_0000b	Address control register low 8 bits
0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD4	SPROG_RDATA	R	0000_0000b	Information block/system block data read register

SPROG_ADDR_H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The system and information modules use bits[7:6] and bit0 of this register Bit[7:6]: block selection when reading data indirectly 10: Select system block, multiplexed to read data indirectly 01: Select information block, multiplexed to read data indirectly 11/00: reserved; {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} address system and information address configuration

SPROG_ADDR_L(CFH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

SPROG_CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x88: Read data indirectly;

SPROG_RDATA (D4H) Information block/system block data read register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Indirectly read the data in the information block

3.2. RAM

There are 256 Bytes internal, the address is 00H~FFH, including working registers group, bit addressing areas, buffers and SFR, the buffer contain the stack area.

Internal low 128 Bytes: 00H~7FH has 128 Bytes. Read and write data by immediate addressing or indirect addressing.

Internal high 128 Bytes: 80H~FFH has 128 Bytes. Read and write data only by immediate addressing or indirect addressing.

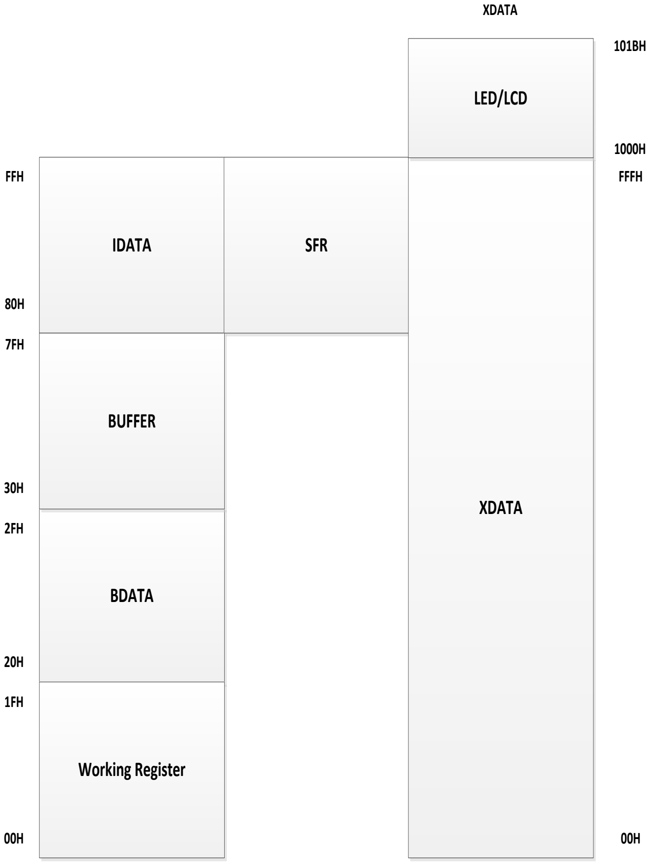
Special function register SFR: the address is 80H~FFH, Read and write data only by direct addressing.

Xdata have 4K Bytes, the address is 0000H~0FFFH, users can use this area completely. To read and write data through the data pointer or working registers group addressing mode.

LED/LCD storage RAM occupies XRAM, the address is 1000~101BH. This area is the LED display buffer, and the display content is modified by changing the area data

Note reserved stack space when writing a program, in order to avoid stack overflow and program goes wrong. Stack first address automatically assigned by program, when programming with C language, but it must be stored in data or idata. KEIL stack can be set in the first address in STARTUP.A51

RAM address space allocation map



RAM	(MSB)							(LSB)	
7FH									Buffer
2FH	7F	7E	7D	7C	7B	7A	79	78	Bit addressing area
2EH	77	76	75	74	73	72	71	70	
2DH	6F	6E	6D	6C	6B	6A	69	68	
2CH	67	66	65	64	63	62	61	60	
2BH	5F	5E	5D	5C	5B	5A	59	58	
2AH	57	56	55	54	53	52	51	50	
29H	4F	4E	4D	4C	4B	4A	49	48	
28H	47	46	45	44	43	42	41	40	
27H	3F	3E	3D	3C	3B	3A	39	38	
26H	37	36	35	34	33	32	31	30	
25H	2F	2E	2D	2C	2B	2A	29	28	
24H	27	26	25	24	23	22	21	20	
23H	1F	1E	1D	1C	1B	1A	19	18	
22H	17	16	15	14	13	12	11	10	
21H	0F	0E	0D	0C	0B	0A	09	08	
20H	07	06	05	04	03	02	01	00	
1FH 18H	3 groups								Working register area
17H 10H	2 groups								
0FH 08H	1 groups								
07H 00H	0 groups								

address allocation map for each bit addressing area

The following table lists the methods to get value in the three parts of RAM:

DATA	MOV A,direct
	MOV direct,A
	MOV direct,#data
	MOV direct1,direct2
	MOV Rn,direct
	MOV direct,Rn

IDATA	MOV A,@Ri
	MOV @Ri,A
	MOV direct,@Ri
	MOV @Ri,direct
	MOV @Ri,#data

XDATA	MOVX @DPTR,A MOVX A,@DPTR

RAM value instruction table

In the above table, n ranges from 0 to 7, and i ranges from 0 to 1.

3.3. SFR Table

Address	Name	RW	Reset	Description
0x80	DATAB	RW	1111_1111b	PB data register
0x81	SP	RW	0000_0111b	Stack pointer register
0x82	DPL	RW	0000_0000b	Data pointer register0 low 8-bit
0x83	DPH	RW	0000_0000b	Data pointer register0 high 8-bit
0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register
0x85	TIMER3_SET_H	RW	0000_0000b	TIMER3 count value configuration register, high 8 bits
0x86	TIMER3_SET_L	RW	0000_0000b	TIMER3 count value configuration register, low 8 bits
0x87	PCON	RW	xxxx_xxx0b	Idle mode 1 select register
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8-bit
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8-bit
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8-bit
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8-bit
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register
0x90	DATAC	RW	1111_1111b	PC port data register
0x91	WDT_CTRL	RW	xxxx_x000b	WDT timing overflow control register
0x92	WDT_EN	RW	0000_0000b	WDT timing enable register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 count value configuration register, high 8 bits
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 count value configuration register, low 8 bits
0x96	REG_ADDR	RW	0000_0000b	Second address bus register
0x97	REG_DATA	RW	0000_0000b	Second data read and write bus register
0x98	UART2_STATE	R/RW	x000_0000b	UART2 status flag register
0x99	PWM0_L_L	RW	0000_0000b	PWM0 low level control register (low 8-bit)
0x9A	PWM0_L_H	RW	0000_0000b	PWM0 low level control register (high 8-bit)
0x9B	PWM0_H_L	RW	0000_0000b	PWM0 high level control register (low 8-bit)
0x9C	PWM0_H_H	RW	0000_0000b	PWM0 high level control register (high 8-bit)
0x9D	PWM1_L_L	RW	0000_0000b	PWM1 low level control register

				(low 8-bit)
0x9E	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8-bit)
0x9F	PWM1_H_L	RW	0000_0000b	PWM1 high level control register (low 8-bit)
0xA0	P2_XH	RW	1111_1111b	MOVX @Ri, A operation pdata address high 8 bits
0xA1	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8-bit)
0xA2	PWM2_L_L	RW	0000_0000b	PWM2 low level control register (low 8-bit)
0xA3	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8-bit)
0xA4	PWM2_H_L	RW	0000_0000b	PWM2 high level control register (low 8-bit)
0xA5	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8-bit)
0xA6	PWM3_L_L	RW	0000_0000b	PWM3 low level control register (low 8-bit)
0xA7	PWM3_L_H	RW	0000_0000b	PWM3 low level control register (high 8-bit)
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xA9	PWM3_H_L	RW	0000_0000b	PWM3 high level control register (low 8-bit)
0xAA	PWM3_H_H	RW	0000_0000b	PWM3 high level control register (high 8-bit))
0xAD	SYS_CLK_CFG	RW	xxx0_1000b	System clock configuration register
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
0xB0	DATAE	RW	1111_1111b	PE data register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000b	LED period configuration register
0xB4	LED2_WIDTH	RW	0000_0000b	LED dot matrix drive mode cycle configuration register
0xB5	SPI_CFG1	RW	0001_0101b	SPI control register 1
0xB6	SPI_CFG2	RW	x001_1000b	SPI control register 2
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xB9	DP_CON1	RW	x000_0000b	LCD contrast configuration register
0xBA	UART2_BDL	RW	0000_0000b	UART2 baud rate control register

0xBB	UART2_CON1	RW	x000_0000b	UART2 mode control register 1
0xBC	UART_IO_CTRL1	RW	xx00_0000b	UART pin enable register
0xBD	UART2_BUF	RW	1111_1111b	UART2 data registerv
0xBE	SPI_STATE	RW	xxxx_x001b	SPI status flag register
0xBF	SPI_SIPD	RW	0000_0000b	SPI data register
0xC0	DATAF	RW	1111_1111b	PF data register
0xC1	ADC_SPT	RW	0000_0000b	ADC sample time configuration register
0xC2	UART_IO_CTRL	RW	xxxx_x000b	UART TXD/RXD pin exchange register
0xC3	ADC_SCAN_CFG	RW	x000_0000b	ADC scan configuration register
0xC4	ADCCKC	RW	0000_0000b	ADC clock and filter configuration register
0xC5	ADC_RDATAH	R	xxxx_0000b	ADC scan result register high 4 bits
0xC6	ADC_RDATAL	R	0000_0000b	ADC scan result register low 8 bits
0xC7	EXINT_STAT	RW	0000_0000b	External Interrupt status register
0xC8	DATAG	RW	xxxx_1111b	PG data register
0xCA	PULL_I_SELA_L	RW	0000_0000b	Pull-up current source size selection register
0xCE	SPROG_ADDR_H	RW	0000_0000b	Address control register
0xCF	SPROG_ADDR_L	RW	0000_0000b	Address control register low 8 bits
0xD0	PSW	R/RW	0000_0000b	Program status word register
0xD1	SPROG_DATA	RW	0000_0000b	Write data register
0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD3	SPROG_TIM	RW	1101_1101b	Erase time control register
0xD4	SPROG_RDATA	R	0000_0000b	Information block/system block data read register
0xD5	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/buck interrupt status register
0xD6	UART1_BDL	RW	0000_0000b	UART1 baudrate control register
0xD7	UART1_CON1	RW	x000_0000b	UART1 mode control register 1
0xD8	DATAH	RW	1111_1111b	PH data register
0xD9	UART1_CON2	RW	xx00_1100b	UART1 mode control register 2
0xDA	UART1_STATE	RW	x000_0000b	UART1 status flag register
0xDB	UART1_BUF	RW	1111_1111b	UART1 data register
0xDC	UART0_BDL	RW	0000_0000b	UART0 baudrate control register
0xDD	UART0_CON1	RW	x000_0000b	UART0 mode control register 1
0xDE	UART0_CON2	RW	xx00_1100b	UART0 mode control register 2
0xDF	UART0_STATE	RW	x000_0000b	UART0 status flag register
0xE0	ACC	RW	0000_0000b	Accumulator

0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE2	UART0_BUF	RW	1111_1111b	UART0 data register
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC send and receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit and receive data buffer register
0xEA	TRISA	RW	xxxx_1111b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xED	UART2_CON2	RW	xx00_1100b	UART2 mode control register 2
0xEE	TRISE	RW	1111_1111b	PE direction register
0xEF	TRISF	RW	1111_1111b	PF direction register
0xF0	B	RW	0000_0000b	B register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF2	TRISG	RW	xxxx_1111b	PG direction register
0xF4	IPL2	RW	0000_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xF7	TRISH	RW	1111_1111b	PH direction register
0xF8	DATAA	RW	xxxx_1111b	PA data register
0xFA	PWM_INT_CTRL	RW	xxxx_xx00b	PWM interrupt enable control register

Note:

1. Registers whose addresses end in 8 or 0 can be bit-operated, for example, registers 0x80 and 0x88.
2. Reset value: reset value of different modes (8 reset modes: power-on reset, power-off reset, programming reset, software reset, modify configuration reset, watchdog timer overflow reset, PC pointer overflow reset, ROM address jump reset).
3. 'x' : indefinite, reserved bit.
4. R: read only; RW: Read and write.
5. the reserved register and register reserved bits, forbid write operations, otherwise may cause chip abnormalities.

3.4. Secondary Bus Register Table

The BF7515CM44-LJTX series supports expanded secondary bus registers for expanding more register functions. Just write the address of the secondary bus register to be accessed into REG_ADDR, and then access the corresponding secondary bus register through the REG_DATA register. It is recommended that when reading and writing secondary bus registers, first EA = 0, and then EA = 1 after the operation is completed. Prevent other interrupts or operations from modifying the address or data of the secondary bus register.

Secondary bus					
Address	**Name**	**Bit**	**RW**	**Description**	**Reset**
0x96	REG_ADDR	<7:0>	RW	Second address bus register	0x00
0x97	REG_DATA	<7:0>	RW	Second data read and write bus register	0x00

Addr	Name	RW	Reset	Description
0x00	CFG0_REG	R	1111_1111b①	Configuration word register 0
0x01	CFG1_REG	R	0110_0100b①	Configuration word register 1
0x02	CFG2_REG	R	0001_1111b①	Configuration word register 2
0x03	CFG3_REG	R	1111_1111b①	Configuration word register 3
0x04	CFG4_REG	R	0010_1101b①	Configuration word register 4
0x05	CFG5_REG	R	1100_1001b①	Configuration word register 5
0x06	CFG6_REG	R	0011_1111b①	Configuration word register 6
0x07	CFG7_REG	R	0001_1111b①	Configuration word register 7
0x08	CFG8_REG	R	1111_1111b①	Configuration word register 8
0x09	CFG9_REG	R	1111_1111b①	Configuration word register 9
0x0A	CFG10_REG	R	1111_1111b①	Configuration word register 10
0x0B	CFG11_REG	R	1111_1111b①	Configuration word register 11
0x0C	CFG12_REG	R	0111_1111b①	Configuration word register 12
0x0D	CFG13_REG	R	0000_0111b①	Configuration word register 13
0x0F	RST_STAT	RW	0000_0010b②	Reset flag register
0x17	PU_PA	RW	xxxx_0000b	PA port pull-up resistor control register
0x18	PU_PB	RW	0000_0000b	PB port pull-up resistor control register
0x19	PU_PC	RW	0000_0000b	PC port pull-up resistor control register
0x1B	PU_PE	RW	0000_0000b	PE port pull-up resistor control register
0x1C	PU_PF	RW	0000_0000b	PF port pull-up resistor control register
0x1D	PU_PG	RW	xxxx_0000b	PG port pull-up resistor control register
0x1E	PU_PH	RW	0000_0000b	PH port pull-up resistor control register
0x1F	LCD_IO_SEL_1	RW	0000_0000b	LCD_SEG0-7 port select configuration register
0x20	LCD_IO_SEL_2	RW	0000_0000b	LCD_SEG8-15 port select configuration register

0x21	LCD_IO_SEL_3	RW	0000_0000b	LCD_SEG16-23 port select configuration register
0x22	LCD_IO_SEL_4	RW	xxxx_0000b	LCD_SEG24-27 port select configuration register
0x23	COM_IO_SEL	RW	0000_0000b	COM select configuration register
0x24	SEG_IO_SEL	RW	0000_0000b	LED_SEG0-7 port select configuration register
0x25	ODRAIN_EN	RW	xxxx_0000b	PC4/5/PE4/5 open drain output enable register
0x2A	ADC_IO_SEL0	RW	x000_0000b	ADC function selection register
0x2C	SEL_LVDT_VTH	RW	xxxx_x000b	LVDT threshold selection register
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register
0x30	IDLE_WAKE_CFG	RW	xxxx_x111b	System wake up configuration register
0x31	LED_DRIVE	RW	xxxx_0000b	LED port drive capability configuration register
0x32	ADC_CFG_SEL	RW	x000_0000b	ADC configuration register
0x33	PWM_IO_SEL	RW	0000_0000b	PWM port selection register
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register 1
0x35	PERIPH_IO_SEL2	RW	0000_0000b	External port function selection register 2
0x36	PERIPH_IO_SEL3	RW	1xxx_xxxxb	External port function selection register 3
0x37	PERIPH_IO_SEL4	RW	0xxx_x000b	External port function selection register 4
0x38	PERIPH_IO_SEL5	RW	0000_0000b	External port function selection register 5
0x39	EXT_INT_CON1	RW	0101_0101b	External interrupt configuration register 1
0x3A	EXT_INT_CON2	RW	xxxx_x001b	External interrupt configuration register 2
0x3E	SPI_TX_START_ADDR	RW	0000_0000b	SPI High-speed mode send buffer first address
0x3F	SPI_RX_START_ADDR	RW	0000_0000b	SPI high-speed mode receive buffer first address
0x40	SPI_NUM_L	RW	0000_0000b	SPI high-speed mode data cache address number low 8 bits
0x41	SPI_NUM_H	RW	xxxx_0000b	SPI high-speed mode data cache address number high 4 bits
0x42	ADC_CFG_SEL1	RW	xx00_0010b	ADC comparator offset cancellation selection register
0x50	IIC_FIL_MODE	RW	xxxx_xx10b	IIC filter selection register
0x53	ADC_IO_SEL1	RW	0000_0000b	ADC select enable register 1
0x54	ADC_IO_SEL2	RW	0000_0000b	ADC select enable register 2
0x55	ADC_IO_SEL3	RW	0000_0000b	ADC select enable register 3
0x56	ADC_IO_SEL4	RW	0000_0000b	ADC select enable register 4
0x57	ADC_IO_SEL5	RW	xxx0_0000b	ADC select enable register 5

0x58	LED_IO_START	RW	xxxx_x000b	LED scan start selection register
0x59	PWM_IO_SEL1	RW	xxxx_0000b	PWM port selection register 1
0x5A	FLASH_BOOT_EN	RO	xxxx_xxx0b	BOOT mode status register
0x5B	EEP_SELECT	RW	xxxx_xxx0b	DATA area selection register
0x60	PWM0_POLA_SEL	RW	xxx0_0000b	PWM0 polarity selection register
0x61	PWM1_POLA_SEL	RW	xxx0_0000b	PWM1 polarity selection register
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register
0x65	SEL_LVDT_DELAY	RW	xxxx_xx00b	LVDT delay control register
0x66	BOR_SEL	RW	xxxx_0000b③	BOR control register
0x67	UART_BD_EXT	RW	xxxx_xxx0b	UART0/1/2 baud rate configuration extension bit register
0x68	SPI_IO_SEL	RW	xxxx_xx00b	SPI communication port selection register
0x69	SPI_MCLK_MOD	RW	xxxx_xxx0b	SPI master mode receiver clock selection register
0x6A	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x6B	ROM_OFFSET_L	R	0000_0000b	Address offset of CODE area, low 8 bit
0x6C	ROM_OFFSET_H	R	0000_0000b	Address offset of CODE area, high 8 bit

Note:

1. Registers whose addresses end with 8 or 0 can be bit-operated.
2. R: read-only; RW: Read and write.
3. 'x' : indeterminate, reserved bit.
4. Do not write the reserved registers and reserved bits of registers. Otherwise, chip exceptions may occur.
5. ①: The reset value is the default value after power-on reset. The global reset value is the factory calibration value, which can be read by referring to 3.1.1.
6. ②: Reset to 1 after power-on. Other resets: Reset to 0 after power-on and 1 after corresponding reset.
7. ③: The register is reset after power-on. Other resets do not change the configuration value.

4. Register Summary

4.1. SFR register Details

DATAB (80H) PB data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB data register, configurable PB group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

SP (81H) Stack pointer register

Bit number	7	6	5	4	3	2	1	0
Symbol	SP[7:0]							
R/W	R/W							
Reset value	7							

DPL (82H) Data pointer register0 low 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPL[7:0]							
R/W	R/W							
Reset value	0							

DPH (83H) Data pointer register0 high 8-bit

Bit number	7	6	5	4	3	2	1	0
Symbol	DPH[7:0]							
R/W	R/W							
Reset value	0							

TIMER3_CFG (84H) TIMER3 configuration register

Bit number	7~3	2	1	0
Symbol	-	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
2	TIMER3_CLK_SEL	TIMER3 timing clock selection register 1: Select clk_24m/4; 0: Select clk_24m/12.

1	TIMER3_RLD	TIMER3 auto reload enable register 1: Auto reload mode; 0: Manual reload mode.
0	TIMER3_EN	TIMER3 count enable register Configure 1 to start timing, configure 0 to stop timing In manual reload mode, the hardware will automatically clear this register after the timing is completed. Configure the register during the scan process to re-count.

TIMER3_SET_H (85H) TIMER3 count value configuration register, high 8-bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER3_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER3_SET_H[7:0]	TIMER3 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER3_SET_L (86H) TIMER3 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER3_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER3_SET_L[7:0]	TIMER3 count value configuration register, low 8 bits, the register will re-count when configured during scanning.

PCON(87H) Idle mode 1 select register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	IM1_EN
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
7~1	--	Reserve
0	IM1_EN	Idle Mode 1 Enable 1: Idle mode 1; 0: Active mode, automatically cleared after wake-up Note: The software delay must be ≥100μs after wake-up,

		otherwise the wake-up function is abnormal

TCON (88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable, when set to1, start Timer1, or start Time0 mode three, TH0 count.
5	TF0	Timer 0 overflow flag, set by hardware when Timer0 overflows.
4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.
3	IE1	External interrupt 1 flag bit, set by hardware, cleared by software.
1	IE0	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
0, 2	--	Reserved

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description
7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer 1 mode select Bit 00 = Mode 0 - 13-bit timer 01 = Mode 1 - 16-bit timer 10 = Mode 2 - 8-bit timer with automatic reloading of initial value 11 = Mode 3 - Two 8-bit timers
1~0	M0[1:0]	Timer 0 mode select Bit 00 = Mode 0 - 13-bit timer 01 = Mode 1 - 16-bit timer 10 = Mode 2 - 8-bit timer with automatic reloading of initial value 11 = Mode 3 - Two 8-bit timers

TL0 (8AH) Timer 0 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0

Symbol	TL0[7:0]
R/W	R/W
Reset value	0

TL1 (8BH) Timer 1 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH0 (8CH) Timer 0 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

TH1 (8DH) Timer 1 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

SOFT_RST (8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	SOFT_RST[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SOFT_RST[7:0]	Soft reset register, only when the register value is 0x55, the software reset is generated

DATAC (90H) PC port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC port data register, you can configure the output level when the IO port of the PC group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

WDT_CTRL (91H) WDT timing overflow control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	WDT_TIME_SEL	WDT timing overflow control register, the timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

WDT_EN (92H) WDT timing enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	WDT_EN	WDT timer enable configuration register, when the configuration value is 0x55, the watchdog is closed

TIMER2_CFG (93H) TIMER2 configuration register

Bit number	7~4	3	2	1	0
Symbol	-	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
3	TIMER2_CNT_MOD	TIMER2 counting step mode selection register 1: The counting step is 65536 clocks 0: The counting step is one clock
2	TIMER2_CLK_SEL	TIMER2 clock selection register 1: select XTAL32.768kHz/4MHz 0: select LIRC
1	TIMER2_RLD	TIMER2 auto reload enable register 1: Auto reload mode 0: manual reload mode
0	TIMER2_EN	TIMER2 count enable register: Configure 1 to start timing, configure 0 to stop timing; In manual reload mode, the hardware will automatically clear this register after the count is completed, stop

		counting, and in automatic reload mode, the enable register will be maintained after the count is completed, and it will automatically restart; Counting from zero, no matter which mode, if this register is set to 1 during the counting process, it will start counting from zero.

TIMER2_SET_H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_H[7:0]	TIMER2 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER2_SET_L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will re-count when configured during scanning

REG_ADDR (96H) Secondary bus address configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	REG_ADDR							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	REG_ADDR	Secondary bus Address configuration register: When operating the secondary bus register, it is recommended that RW secondary bus register first, EA = 0, then EA = 1, after the operation is completed, to prevent other interrupts or operations from modifying the secondary bus register Address or data

REG_DATA (97H) Second data read and write bus register

Bit number	7	6	5	4	3	2	1	0

Symbol	REG_DATA
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	REG_DATA	Secondary bus data RW register: When RW secondary bus register is recommended, EA = 0 first, then EA = 1, after the operation is completed, to prevent other interrupts or operations from modifying the address or data of the secondary bus register

UART2_STATE (98H) UART2 status flag register

Bit number	7	6	5	4
Symbol	-	UART2_R8	UART2_T8	TI2
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI2	UART2_RO	UART2_F	UART2_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART2_R8	The 9th data of the receiver, read only
5	UART2_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI2	Send interrupt mark: 1: Send buffer is empty 0: Send buffer is full, software write 0 to clear, write 1 invalid
3	RI2	Receive interrupt flag: 1: Receive buffer is full 0: Receive buffer is empty, software write 0 to clear, write 1 invalid
2	UART2_RO	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART2_F	Frame error flag: 1: Frame error detected 0: Frame error not detected, software write 0 to clear, write 1 is invalid

0	UART2_P	Parity error flag: 1: Receiver parity error 0: Parity is correct, software write 0 to clear, write 1 is invalid

PWM0_L_L (99H) PWM0 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_L_H (9AH) PWM0 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_H_L (9BH) PWM0 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_H_H (9CH) PWM0 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_L_L (9DH) PWM1 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_L_H (9EH) PWM1 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_H_L (9FH) PWM1 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

P2_XH (A0H) MOVX @Ri, A operation pdata address high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	P2_XH	When using MOVX @Ri, A instruction, when operating pdata area, P2_XH needs to be cleared to 0

PWM1_H_H (A1H) PWM1 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM2_L_L (A2H) PWM2 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM2_L_H (A3H) PWM2 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM2_H_L (A4H) PWM2 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM2_H_H (A5H) PWM2 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM3_L_L (A6H) PWM3 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	0

PWM3_L_H (A7H) PWM3 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

IEN0(A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit. 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer 1 overflow interrupt enable bit: 0: Disable timer 1 (TF1) to apply for interrupt; 1: Allow TF1 flag bit to request interrupt.
2	EX1	INT_EXT1 enable bit: 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 overflow interrupt enable bit: 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit: 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

PWM3_H_L (A9H) PWM3 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM3_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM3_H_H (AAH) PWM3 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0

Symbol	PWM3_H_H[7:0]
R/W	R/W
Reset value	0

SYS_CLK_CFG (ADH) System clock configuration register

Bit number	7~5	4	3	2	1	0
Symbol	-	IM0_EN	PLL_CLK_SEL			PD_SYS_CLK
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	1	0	0	0

Bit number	Bit symbol	Description
7~5	--	Reserved
4	IM0_EN	Idle mode 0 enable: 1: The chip enters the Idle mode 0 0: The chip exits the Idle mode 0
3~1	PLL_CLK_SEL	PLL clock divider selection register: 000/100: 12MHz; 001/101: 8MHz; 010/110: 4MHz; 011/111: 1MHz
0	PD_SYS_CLK	Core clock enable: 0: Turn on the core clock 1: Turn off the core clock

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	INT_PWM1_STAT	PWM1 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM1 channel 1: Interrupt is valid; 0: Interrupt is invalid
6	INT_TIMER3_STAT	TIMER3 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER3_CFG,

		1: Interrupt is valid; 0: Interrupt is invalid
5	INT08_STAT	INT08 port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT08_IO_SEL=0 1: Interrupt is valid 0: Interrupt is invalid
4	INT_WDT_STAT	WDT interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing WDT_CTRL, 1: Interrupt is valid 0: Interrupt is invalid
3	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER2_CFG, 1: Interrupt is valid 0: Interrupt is invalid
2	INT_PWM0_STAT	PWM0 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM0 channel 1: Interrupt is valid; 0: Interrupt is invalid
1	INT_LCD_STAT	LCD interrupt status mark, write 0 to clear this bit, write SCAN_START operation can also be cleared, 1: Interrupt is valid 0: Interrupt is invalid
0	INT_LED_STAT	LED interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START, 1: Interrupt is valid 0: Interrupt is invalid

SCAN_START (AFH) LCD, LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LCD, LED scan on register: 1: Scan on; 0: Scan off

DATAE (B0H) PE port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PE data register, you can configure the output level of PE group IO port as GPIO port, the read value is the current level state of IO port (input) or configure output value (output).

DP_CON (B1H) LCD, LED control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	IO_ON	DUTY_SEL			DPSEL	SCAN_MODE	COM_MOD
R/W	-	R/W	R/W			R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports: 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LED dot matrix drive mode dot matrix selection configuration register Bit[1:0]: 00: 4x5 dot matrix; 01: 5x6 dot matrix 10: 6x7 dot matrix; 11: 7x8 dot matrix Bit [2]: 0: LED0 as the starting port 1: 4x5 dot matrix—Enable with LED3 (as the starting port) LED row and column drive mode single SEG port conduction duty cycle configuration register: 0: 1/8 duty cycle 1: 2/8 duty cycle 2: 3/8 duty cycle 3: 4/8 duty cycle 4: 5/8 duty cycle 5: 6/8 duty cycle 6: 7/8 duty cycle 7: 8/8 duty cycle LCD drive mode duty cycle configuration register 000: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG) COM port: COM0-3, SEG port: SEG0-23 001: 1/8 duty cycle, 1/4 bias (8 COM X 16/24SEG) COM port: COM0-7, SEG port: SEG0-23 010: 1/4 duty cycle, 1/3 bias (4 COM X 20/28 SEG)

		COM port: COM0-3, SEG port: SEG0-23, COM4-7 shared as SEG24-27 011: 1/5 duty cycle, 1/3 bias (5 COM X 19/27 SEG) COM port: COM0-4, SEG port: SEG0-23, COM5-7 shared as SEG25-27 100: 1/6 duty cycle, 1/3 bias (6 COM X 18/26 SEG) COM: COM0-5, SEG: SEG0 -23, COM6-7 shared as SEG26-SEG27 101: 1/6 duty cycle, 1/4 bias (6 COM X 18/26 SEG) COM port: COM0-5 SEG port: SEG0-23, COM6-7 shared as SEG26-SEG27 Others: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG) COM: COM0-3, SEG: SEG0-23
2	DPSEL	LCD, LED selection control bit 0: Select LCD driver, LED driver is invalid 1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration 1: Cycle scan mode 0: Interrupt scan mode
0	COM_MOD	High-current IO port driver enable 1: The COM port function is locked and works as a high-current IO port; 0: The COM port function is not locked and can be configured as other functions; When the COM port function is locked to the high-current IO port, configure the GPIO register output drive timing, LED/LCD scan configuration is invalid

DP_MODE (B2H) LCD, LED mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_CKSEL		LCD_RSEL	LCD_FCSEL		LCD_RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	LED_MOD	LED drive mode selection register 1: Serial dot matrix scanning 0: Row and column matrix scan
6~5	LCD_CKSEL	LCD clock selection register 10/11: select RC1M

		01: Select XTAL 00: Select LIRC32kHz
3~2	LCD_FCSEL	Charge time control bit 00: 1/8 COM of LCD period; 01: 1/16 COM of LCD period; 10: 1/32 COM of LCD period; 11: 1/64 COM of LCD period
4	LCD_RSEL	LCD bias resistance selection control bit 0: The sum of LCD bias resistance is 225k; 1: The sum of LCD bias resistance is 900k
1~0	LCD_RMOD	Drive mode selection bit 00: Traditional resistance mode (slow charging mode), the total bias resistance is 225k/900k, when LCD_RSEL = 0, the total LCD bias resistance is 225K, when LCD_RSEL = 1, the total LCD bias resistance is 900K 01: Traditional resistance mode (fast charging mode), the total bias resistance is 60k 10/11: Fast and slow charging automatic switching mode, the total bias resistance is automatically switched between 60k and 225k/900k

SCAN_WIDTH (B3H) LED period configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Under LED matrix drive mode, corresponding to the scan time of a single COM port In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the first segment of the lamp cycle configuration: period=(scan_width+1)*16us, the support configuration range is 0.016~4.096ms; When on-time 1<on-time 2, the scan time of this group is on-time 2.In LCD drive mode, the corresponding single COM port scan time: period=(scan_width+1)*64us, support configuration range 0.064~4.096ms, high two digits Reserved Note: In this mode, this register is only applicable to the LCD selection clock CLK_1M mode, the slowest LCD frame rate in

		other clock modes is 64Hz (8*24)

LED2_WIDTH (B4H) LED dot matrix drive mode cycle configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the second stage of lamp cycle configuration period=(led2_width+1)*16us Note: This register is only applicable to LED dot matrix drive mode: when the on time 1 is greater than the on time 2, the scan time of this group is on time 1.

SPI_CFG1 (B5H) SPI control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	RX_IE	SPI_EN	TX_IE	MSTR	CPOL	CPHA	LSBFE	CS_N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
7	RX_IE	Receive enable- SPI receive buffer is full (SPRF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
6	SPI_EN	SPI enable: 1: module enable open; 0: module enable close
5	TX_IE	Transmit enable - SPI transmit buffer empty (SPTEF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
4	MSTR	Master-slave mode selection 1: Master mode; 0: Slave mode
3	CPOL	SCLK active level selection 1: Active low; 0: Active high
2	CPHA	SCLK phase selection 1: Send data at the first valid clock edge 0: Sample data at the first valid clock edge
1	LSBFE	LSB first (shifter direction) 1: SPI serial data transmission starts from the lowest bit

		0: SPI serial data transmission starts from the highest bit
0	CS_N	Chip select signal: 0: Pull down CS 1: Pull up CS

SPI_CFG2 (B6H) SPI control register 2

Bit number	7	6	5	4
Symbol	-	FEEDBACK	HSPEED_START	HALF_FUPLEX
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1
Bit number	3	2	1	0
Symbol	BIDIR_SELECT	SPR		
R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0

Bit number	Bit symbol	Description
6	FEEDBACK	Send the received data to the master\slave 1: Send the received data to the master\slave 0: Send the data written by MCU to the master\slave
5	HSPEED_START	The high-speed SPI communication mode is turned on and the hardware is automatically pulled down after the work is completed 1: High-speed SPI communication mode is on 0: High-speed SPI communication mode is off. In high-speed SPI mode, whether in slave or master mode, the chip select signal cannot be pulled high, which will cause the data sent by SPI to be lost
4	HALF_FUPLEX	Half-duplex mode selection: 1: Select half-duplex mode; 0: Select full-duplex mode
3	BIDIR_SELECT	Half-duplex mode, transmission and reception direction selection 1: Send; 0: Receive
2~0	SPR	SPI baud rate coefficient, up to 2MHz: 000: spi_clk/2; 001: spi_clk /4; 010: spi_clk/6; 011: spi_clk /8; 100: spi_clk/10; 101: spi_clk /12; 110: spi_clk/14; 111: spi_clk /16;

IPL0 (B8H) Interrupt priority register0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0

R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1 (Timer1 interrupt) priority selection bit. 0: Timer1 is low priority; 1: Timer1 is 1high priority
2	PX2	INT_EXT1 interrupt priority selection bit. 0: INT_EXT1 is low priority; 1: INT_EXT1 is high priority
1	PT0	TF0 (Timer0 interrupt) priority selection bit. 0: Timer0 is low priority; 1: Timer0 is high priority
0	PX0	INT_EXT0 interrupt priority selection bit. 0: INT_EXT is low priority; 1: INT_EXT is high priority

DP_CON1 (B9H) LCD contrast configuration register

Bit number	7	6	5	4
Symbol	-	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	VOL			
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	TRI_COM_INV	LED matrix 4*4 mode COM port reverse selection register In 4*4 mode, 1: Output high when COM is selected 0: Output low when COM is selected
5	MATRIX_MOD	LED matrix 4*4 mode selection register: 1: Select 4*4 mode, LED0~LED3 correspond, COM0~COM3 port selection, LED4~LED7 correspond, SEG0~SEG3 port selection; 0: Do not select 4*4 mode
4	PD_LCD_POWER	LCD contrast control enable bit: 0: Turn off LCD contrast control 1: Turn on LCD contrast control
3~0	VOL	LCD contrast control bit: 0000: VLCD = 0.53VDD; 0001: VLCD = 0.56VDD; 0010: VLCD = 0.59VDD; 0011: VLCD = 0.63VDD; 0100: VLCD = 0.66VDD; 0101: VLCD = 0.69VDD;

		0110: VLCD = 0.72VDD; 0111: VLCD = 0.75VDD; 1000: VLCD = 0.78VDD; 1001: VLCD = 0.81VDD; 1010: VLCD = 0.84VDD; 1011: VLCD = 0.88VDD; 1100: VLCD = 0.91VDD; 1101: VLCD = 0.94VDD; 1110: VLCD = 0.97VDD; 1111: VLCD = 1.00VDD

UART2_BDL (BAH) UART2 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART2_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART2_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register UART_BD_EXT=0, Baud_Mod = {UART2_BDH[1:0], UART2_BDL}; UART_BD_EXT=1, Baud_Mod= {UART2_BD_ADD[1:0], UART2_BDH[1:0], UART2_BDL}; When Baud_Mod=0, the baud rate clock is not generated; When Baud_Mod>1, the baud rate = BUSCLK/(16xBaud_Mod)

UART2_CON1 (BBH) UART2 mode control register 1

Bit number	7	6	5	4
Symbol	-	UART2_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART2_ENABLE	Module enable 1: Module is enabled; 0: Module is turned off
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is turned on; 0: Receiver is turned off
4	MULTI_MODE	Multiprocessor communication mode

		1: Mode is enabled; 0: Mode is disabled
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled; 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check; 0: Even check

UART_IO_CTRL1 (BCH) UART pin enable register

Bit number	7	6	5	4
Symbol	-	-	UART2_RXD_DIASB	UART2_TXD_DIASB
R/W	-	-	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5	UART2_RXD_DIASB	UART2 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
4	UART2_TXD_DIASB	UART2 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled
3	UART1_RXD_DIASB	UART1 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
2	UART1_TXD_DIASB	UART1 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled
1	UART0_RXD_DIASB	UART0 RXD port disabled

		0: RXD pin is enabled; 1: RXD pin is disabled
0	UART0_TXD_DIASB	UART0 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled

UART2_BUF (BDH) UART2 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART2_BUF[7:0]							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	UART2_BUF[7:0]	UART2 data register: Reads and returns the content of read-only receive data buffer, writes into write-only transmit data buffer

SPI_STATE (BEH) SPI status flag register

Bit number	7~3	2	1	0
Symbol	-	SPRF	OVERFLOW_RX	SPTEF
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	SPRF	Read buffer full mark, software write 0 to clear 0: In the receive data buffer, no data is available; 1: In the receive data buffer, there is data
1	OVERFLOW_RX	In the normal communication mode, when the receiving overflow is caused by not reading in time, OVERFLOW_RX=1, the signal does not generate an interrupt, only the mark In high-speed SPI communication mode, it is invalid (when the number of received data is equal to the configured {SPI_NUM_H, SPI_NUM_L}, the work will end, SPRF will be set, and a full interrupt will be generated).
0	SPTEF	Send buffer empty mark, write into SPID hardware to clear automatically. In the SPI idle state, the first data written to SPID will be directly stored in the shift register, and the second data written will be loaded into the transmit buffer, and SPTEF will be automatically pulled low. 1: The data cache is empty, data can be written;

		0: The data cache is not empty

SPI_SPID (BFH) SPI port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	SPI_SPID[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPI_SPID[7:0]	SPID reading this register will return the data read from the receive data buffer rx_reg. Writing to this register will write data into the transmit data buffer tx_reg. Data should not be written into the transmit data buffer, unless the SPI transmit buffer empty flag (SPTEF) is set, indicating that there is a certain space in the transmit buffer to queue new transmit bytes. After setting the SPRF and before completing another transmission, you can read data from the SPID at any time. If the data is not read from the receive data buffer before the end of the new transmission, the receive overflow will result and the newly transmitted data will be lost.

DATAF (C0H) PF port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PF data register, you can configure the output level of the PF group IO port as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

ADC_SPT (C1H) ADC sampling time configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT[7:0]	ADC sampling time configuration register Sampling time: t1= (ADC_SPT+1)*4* T_{ADCK}

UART_IO_CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2	1	0
Symbol	-	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
2	UART2_PAD_CHANGE	UART2 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange
1	UART1_PAD_CHANGE	UART1 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange
0	UART0_PAD_CHANGE	UART0 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

ADC_SCAN_CFG (C3H) ADC scan configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADC_ADDR						ADC_START
R/W	-	R/W						R/W
Reset value	-	0						0

Bit number	Bit symbol	Description
6~1	ADC_ADDR	ADC channel address selection register 000000: Corresponding to ADC0; 000001: Corresponding to ADC1; …… 101010: Corresponding to ADC42; 101011: Corresponding to ADC43; 101100: ADC44_VREF. others: Reserved
0	ADC_START	ADC scan open register: 0: ADC module does not scan; 1: ADC module starts to scan ADC_START is set from 0 to 1, ADC starts to scan, after scanning once, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit. The ADC interrupt flag bit needs to be cleared by software. Note: ADC_START is not allowed to be configured during scanning

ADCCKC (C4H) ADC clock and filter configuration register

Bit number	7	6	5	4
Symbol	FILTER_SEL	SAMBG	SAMDEL	

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	ADCCKV		ADCK	
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	FILTER_SEL	ADC filter selection 0: No RC filter added; 1: RC filter added.
6	SAMBG	Sampling timing and comparison timing interval selection 0: interval of 0 T_{ADCK}; 1: interval of 1 T_{ADCK}
5~4	SAMDEL	Sampling delay time selection 00: 0*T_{ADCK}; 01: 2*T_{ADCK}; 10: 4*T_{ADCK}; 11: 8*T_{ADCK}
3~2	ADCCKV	ADC comparator offset cancellation analog input clock 00: 12MHz; 01: 8MHz; 10: 4MHz; 11: 2MHz
1~0	ADCK	ADC clock 00: 8MHz; 01: 6MHz; 10: 4MHz; 11: 3MHz

ADC_RDATAH (C5H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH [3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

ADC_RDATAL (C6H) ADC scan result register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
3~0	ADC_RDATAH[3:0]	ADC scan result register, high 4bit
7~0	ADC_RDATAL[7:0]	ADC scan result register, low 8Bit

EXINT_STAT (C7H) External interrupt status register

Bit number	7	6	5	4
Symbol	INT07_STAT	INT06_STAT	INT05_STAT	INT04_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT03_STAT	INT02_STAT	INT01_STAT	INT00_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	INT0x_STAT (x=7~0)	INT0x port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT0x_IO_SEL=0, 1: Interrupt is valid; 0: Interrupt is invalid

DATAG (C8H) PG port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PG3	PG2	PG1	PG0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	PG data register, you can configure the output level when the IO port of the PG group is used as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output).

SPROG_ADDR_H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Bit[7:6]: block selection when reading data indirectly 10: Select system block, multiplex to read data indirectly (SPROG_CMD=0x88) 01: Select information block, multiplexed to read data indirectly (SPROG_CMD=0x88); 11/00: invalid; In non-Flash_Boot upgrade mode: Bit[6:2]: DATA area (0xFC00~0xFFFF) selection enable

		00000: Select DATA area (0xFC00~0xFFFF), 1024Bytes Other: invalid **1. DATA area (0xFC00~0xFFFF):** config {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} **2. When SPROG_ADDR_H[2]=1, select NVR4:** config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} **3. When SPROG_ADDR_H[2]=0, select NVR3:** config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} Note: In Flash_Boot upgrade mode, { SPROG_ADDR_H, SPROG_ADDR_L} multiplexing all space addresses of CODE

SPROG_ADDR_L(CFH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

PSW (D0H) Program status word register

Bit number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS[1:0]		OV	F1	P
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	CY	Carry flag 0: In arithmetic or logic operation, no carry or borrow occurs 1: In arithmetic or logic operation, a carry or borrow occurs
6	AC	Auxiliary carry flag 0: In arithmetic logic operation, no auxiliary carry or borrow occurs 1: In arithmetic logic operation, an auxiliary carry or borrow occurs
5	F0	0 flag bit. Generic labels available to users.
4~3	RS[1:0]	Working register group selection: Select a valid working register group: RS[1:0] Bank IRAM Area 00 0 0x00-0x07; 01 1 0x08-0x0F;

		10 2 0x10-0x17; 11 3 0x18-0x1F.
2	OV	Overflow flag 0: No overflow occurred; 1: Overflow occurred
1	F1	1 flag.Generic labels available to users.
0	P	Parity bit 0: The number of digits with value 1 in accumulator A is even; 1: The number of digits with a value of 1 in the accumulator A is an odd number.

SPROG_DATA(D1H)Write data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	data to be written

SPROG_CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: page erase Write 0x69: byte burn Write 0x88: read data indirectly; When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9A, enter the Flash Boot upgrade mode; When continuously writing data 0xFE, 0xDC, 0xBA, 0x98, 0x76, exit the Flash Boot upgrade mode When CFG_BOOT_SEL = 3 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered.

SPROG_TIM(D3H) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	1	1	1	0	1

Bit number	Bit symbol	Description

7~5	SPROG_TIM[7:5]	Byte write fixed time is 23.5us
4~0	SPROG_TIM[4:0]	Erase time configuration SPROG_TIM[4:0]=0~31 When the selected address is 0xFC00~0xFFFF: When SPROG_TIM[4:0]=0~9, Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms) When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9, Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time=4.57(ms)

SPROG_RDATA (D4H) Information block/system block data read register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Indirectly read the data in the information block/system block

INT_POBO_STAT (D5H) LVDT boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT boost interrupt status. 1: Boost interrupt is valid; 0: Boost interrupt is invalid.
0	INT_BO_STAT	LVDT buck interrupt status. 1: The buck interrupt is valid; 0: The buck interrupt is invalid

UART1_BDL (D6H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART1_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART1_BDL[7:0]	Baud rate control register Baud rate modulus divisor register, low 8 bits UART_BD_EXT=0, Baud_Mod = {UART1_BDH[1:0], UART1_BDL}; UART_BD_EXT=1, Baud_Mod= {UART1_BD_ADD[1:0], UART1_BDH[1:0], UART1_BDL}; When Baud_Mod=0, the baud rate clock will not be generated. When Baud_Mod>1, baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON1 (D7H) UART1 mode control register

Bit number	7	6	5	4
Symbol	-	UART1_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_ENABLE	Module enable 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi -processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

DATAH (D8H) PH port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PH data register, can configure the output level of PH group IO port as GPIO port, the read value is the current level state of IO port (input) or configure output value (output)

UART1_CON2 (D9H) UART1 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART1_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART1_BD_ADD	The upper 2 bits of the baud rate modulus divisor register. (it is determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Send interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART1_BDH	Baud rate modulus divisor register, high 2 bits

UART1_STATE (DAH) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_R8	The 9th data of the receiver, read only
5	UART1_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI1	Send interrupt mark: 1: The sending buffer is empty

		0: Send buffer is full, software write 0 to clear, write 1 is invalid
3	RI1	Receive interrupt mark: 1: The receive buffer is full 0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART1_RO	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART1_F	Frame error flag 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART1_P	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

UART1_BUF (DBH) UART1 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

UART0_BDL (DCH) UART0 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART0_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART0_BDL[7:0]	Baud rate control register, Baud rate modulus divisor register, low 8 bits UART_BD_EXT=0, Baud_Mod = {UART0_BDH[1:0], UART0_BDL}; UART_BD_EXT=1, Baud_Mod= {UART0_BD_ADD[1:0], UART0_BDH[1:0], UART0_BDL};

		When Baud_Mod=0, the baud rate clock is not generated; when Baud_Mod>1, baud rate = BUSCLK/(16xBaud_Mod)

UART0_CON1 (DDH) UART0 mode control register 1

Bit number	7	6	5	4
Symbol	-	UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_ENABLE	Module enable 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi- processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

UART0_CON2 (DEH) UART0 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART0_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	R/W	R/W	R/W		R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART0_BD_ADD	Baud rate modulus divisor register, high 2 bits (determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Transmit interrupt enable 1: Interrupt enable 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable

		1: Interrupt enable 0: Interrupt disable (used in polling mode)
1~0	UART0_BDH	The upper 2 bits of the baud rate modulus divisor register

UART0_STATE (DFH) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_R8	The 9th data of the receiver, read only
5	UART0_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI0	Send interrupt mark: 1: The sending buffer is empty 0: Send buffer is full, software write 0 to clear, write 1 is invalid
3	RI0	Receive interrupt mark: 1: The receive buffer is full 0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART0_RO	Receive overflow flag: 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART0_F	Frame error flag: 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART0_P	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

ACC (E0H) Accumulator

Bit number	7	6	5	4	3	2	1	0
Symbol	ACC							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	ACC	Accumulator: The destination register is suitable for all arithmetic and logic operations.

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	IE15	External Interrupt4 interrupt flag bit 1: With External Interrupt4 interrupt flag 0: Clear External Interrupt4 interrupt flag
6	IE14	External Interrupt3 interrupt flag bit 1: With External Interrupt3 interrupt flag 0: Clear External Interrupt3 interrupt flag
5	IE13	SPI interrupt flag bit 1: There is SPI interrupt flag 0: Clear SPI interrupt flag
4	IE12	Timer3/PWM1 interrupt flag bit 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag
3	IE11	UART1 interrupt flag bit 1: UART1 interrupt flag is available 0: Clear UART1 interrupt flag
2	IE10	UART0 interrupt flag bit 1: UART0 interrupt flag is available 0: Clear UART0 interrupt flag
1	IE9	LVDT interrupt flag bit 1: LVDT interrupt flag is present 0: LVDT interrupt flag is cleared
0	IE8	UART2 interrupt flag bit 1: UART2 interrupt flag is available 0: Clear LVDT interrupt flag

UART0_BUF (E2H) UART0 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	FF

Bit number	Bit symbol	Description
7~0	--	Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

IICBUF (E4H) IIC send and receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	-	-	IIC_RST	RD_SCL_EN
R/W	-	-	R/W	R/W
Reset value	-	-	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation, 0: IIC module works normally
4	RD_SCL_EN	The host reads the low clock line control bit 1: Enable the host to read and pull down the clock line function, 0: Disable the host read and pull down clock line function
3	WR_SCL_EN	The host writes the low clock line control bit, 1: Enable the function of writing and pulling down the clock line,

		0: Disable the function of writing and pulling down the clock line
2	SCLEN	IIC clock enable bit: 1=clock works normally, 0=lows the clock line
1	SR	IIC conversion rate control bit 1: The conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit: 1: IIC works normally, 0: IIC does not work

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2/PWM0 interrupt enable 1: WDT/Timer2/PWM0 interrupt enable; 0: WDT/Timer2/PWM0 interrupt disable
6	EX6	LED/LCD interrupt enable 1: LED/LCD interrupt enable; 0: LED/LCD interrupt disable
4	EX4	ADC interrupt enable 1: ADC interrupt enable; 0: ADC interrupt disable
3	EX3	IIC interrupt enable 1: IIC interrupt enable; 0: IIC interrupt disable
2	EX2	External Interrupt2 interrupt enable 1: External Interrupt2 interrupt enable; 0: External Interrupt2 interrupt disable
5, 1~0	-	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	EX15	External Interrupt4 enable 1: External Interrupt4 interrupt enable; 0: External Interrupt4 interrupt disable
6	EX14	External Interrupt3 enable 1: External Interrupt3 enable; 0: External Interrupt3 disable
5	EX13	SPI interrupt enable 1: SPI interrupt enable; 0: SPI interrupt disable
4	EX12	Timer3/PWM1 interrupt enable 1: Timer3/PWM1 interrupt enable; 0: Timer3/PWM1 interrupt disable
3	EX11	UART1 interrupt enable 1: UART1 interrupt enable; 0: UART1 interrupt disable
2	EX10	UART0 interrupt enable 1: UART0 interrupt enable; 0: UART0 disable
1	EX9	LVDT interrupt enable 1: LVDT interrupt enable; 0: LVDT interrupt disable
0	EX8	UART2 interrupt enable 1: UART2 interrupt enable; 0: UART2 interrupt disable

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: Indicates that the start bit is detected; 0: Indicates that the start bit is not detected.
6	IIC_STOP	Stop signal flag

		1: Means in the stop state; 0: Means that the stop bit is not detected.
5	IIC_RW	Read and write flag Record the read/write information obtained from the address byte after the last address match, 1: Indicates read operation; 0: Means write operation.
4	IIC_AD	Address data flag 1: Indicates that the most recently received or sent byte is data; 0: Indicates that the most recently received or sent byte is an address.
3	IIC_BF	IICBUF full flag bit: when receiving in IIC bus mode 1: Indicates that the reception is successful and the buffer is full; 0: Indicates that the reception is not completed and the buffer is still empty When sending in IIC bus mode: 1: Indicates that data transmission is in progress (not including the response bit and stop bit), and the buffer is still full; 0: Indicates that the data transmission has been completed (not including the response bit and stop bit), and the buffer is empty.
2	IIC_ACK	Reply flag 1: Indicates an invalid response signal; 0: Indicates an effective response signal.
1	IIC_WCOL	Write conflict flag 1: Indicates that when the IIC is sending the current data, new data is trying to be written into the sending buffer; the new data cannot be written into the buffer; 0: No write conflict occurred.
0	IIC_RECOV	Receive overflow flag 1: Indicates that new data is received when the previous data received by IIC has not been taken away, and the new data cannot be received by the buffer; 0: Indicates that no receive overflow has occurred.

IICBUFFER (E9H) IIC transmit and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							

R/W	R/W
Reset value	0

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	Bit[3]~ Bit[1]: direction of PA3~PA0 port pins 0: PAx port is output; 1: PAx port is input

TRISB (EBH) PB direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PB7~PB0 port pins 0: PBx port is output; 1: PBx port is input

TRISC (ECH) PC direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]:direction of PC7~PC0 port pins 0: PCx port is output; 1: PCx port is input

UART2_CON2 (EDH) UART2 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART2_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART2_BDH	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART2_BD_ADD	The upper 2 bits of the baud rate modulus divisor register.

		(it is determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Send interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART2_BDH	Baud rate modulus divisor register, high 2 bits

TRISE (EEH) PE direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PE7~PE0 port pins 0: PEx port is output; 1: PEx port is input

TRISF (EFH) PF direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PF7~PF0 port pins 0: PFx port is output; 1: PFx port is input

B (F0H) B register

Bit number	7	6	5	4	3	2	1	0
Symbol	B							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	B	B register: the source and destination registers of multiplication and division operations.

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0

Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag 1: WDT/Timer2/PWM0 interrupt flag; 0: Clear WDT/Timer2/PWM0 interrupt flag
6	IE6	LED/LCD interrupt flag 1: With LED interrupt flag; 0: Clear LED interrupt flag
4	IE4	ADC interrupt flag 1: ADC interrupt flag is present; 0: ADC interrupt flag is cleared
3	IE3	IIC interrupt flag 1: IIC interrupt flag is present; 0: IIC interrupt flag is cleared
2	IE2	External Interrupt2 interrupt flag 1: External Interrupt2 interrupt flag; 0: Clear External Interrupt2 interrupt flag
5, 1~0	–	Reserved

TRISG (F2H) PG direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	Bit[3]~ Bit[1]:direction of PG3~PG0 port pins 0: PGx port is output; 1: PGx port is input

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	IPL2.7	External Interrupt4 priority selection bit. 1: External Interrupt4 interrupt is high priority;

		0: External Interrupt4 interrupt is low priority
6	IPL2.6	External Interrupt3 priority selection bit. 1: External Interrupt3 interrupt is high priority; 0: External Interrupt3 interrupt is low priority
5	IPL2.5	SPI priority selection bit. 1: SPI interrupt is high priority; 0: SPI interrupt is low priority
4	IPL2.4	Timer3/PWM1 priority selection bit. 1: Timer3/PWM1 interrupt is high priority; 0: Timer3/PWM1 interrupt is low priority
3	IPL2.3	UART1 priority selection bit. 1: UART1 interrupt is high priority; 0: UART1 interrupt is low priority
2	IPL2.2	UART0 priority selection bit. 1: UART0 interrupt is high priority; 0: UART0 interrupt is low priority
1	IPL2.1	LVDT priority selection bit. 1: LVDT interrupt is high priority; 0: LVDT interrupt is low priority
0	IPL2.0	UART2 priority selection bit. 1: UART2 interrupt is high priority; 0: UART2 interrupt is low priority

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit 1: WDT/Timer 2/PWM0 interrupt is high priority; 0: WDT/Timer 2/PWM0 interrupt is low priority
6	IPL1.6	LED/LCD interrupt priority bit 1: LED/LCD interrupt is high priority; 0: LED/LCD interrupt is low priority
4	IPL1.4	ADC interrupt priority bit 1: ADC interrupt is high priority; 0: ADC interrupt is low priority
3	IPL1.3	IIC interrupt priority bit 1: IIC interrupt is high priority;

		0: IIC interrupt is low priority
2	IPL1.2	External Interrupt2 priority selection bit 1: External Interrupt2 is high priority; 0: External Interrupt2 is low priority
5, 1~0	--	Reserved

TRISH (F7H) PH direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: direction of PH7~PH0 port pins 0: PHx port is output; 1: PHx port is input

DATAA (F8H) PA port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PA3	PA2	PA1	PA0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	PA data register, you can configure the output level of the PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output value (output)

PWM_INT_CTRL (FAH) PWM interrupt enable control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	--	PWM1 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disable
0	--	PWM0 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disable

Note:

4.2. Secondary Bus Registers Details

CFG0_REG (00H) Configuration word register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG1_REG (01H) Configuration word register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	64							

CFG2_REG (02H) Configuration word register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	1F							

CFG3_REG (03H) Configuration word register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG4_REG (04H) Configuration word register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	2D							

CFG5_REG (05H) Configuration word register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	C9							

CFG6_REG (06H) Configuration word register 6

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	3F							

CFG7_REG (07H) Configuration word register 7

Bit number	7	6	5	4	3	2	1	0
Symbol	-							

R/W	R
Reset value	1F

CFG8_REG (08H) Configuration word register 8

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG9_REG (09H) Configuration word register 9

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG10_REG (0AH) Configuration word register 10

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG11_REG (0BH) Configuration word register 11

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	FF							

CFG12_REG (0CH) Configuration word register 12

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	7F							

CFG13_REG (0DH) Configuration word register 13

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	7							

RST_STAT (0FH) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_F	DEBUG_F	SOFT_F	PROG_F	ADDROF_F	BO_F	PO_F	WDTRST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	0: no effect; 1: A reset occurs when the configuration program space jumps
6	DEBUG_F	0: No effect; 1: Trim configuration reset occurred.
5	SOFT_F	0: No effect; 1: Software reset occurred.
4	PROG_F	0: No effect; 1: Program reset occurred.
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred.
2	BO_F	0: No effect; 1: Power_down reset occurred.
1	PO_F	0: No effect; 1: Power_on reset occurred.
0	WDTRST_F	0: No effect; 1: Watchdog timer overflow reset occurred.

PU_PA (17H) PA pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	PA pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB (18H) PB pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PB pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PC (19H) PC pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0

Symbol	-
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	PC pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PE (1BH) PE pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PE pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PF (1CH) PF pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PF pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PG (1DH) PG pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	PG pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PH (1EH) PH pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0

Symbol	-
R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	PH pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

LCD_IO_SEL_1 (1FH) LCD_SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG0-7 port selection configuration register, the corresponding bit is 1 to select SEG port function 1: Select SEGMENT port mode; 0: Select IO port mode

LCD_IO_SEL_2 (20H) LCD_SEG8-15 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG8-15 port selection configuration register, the corresponding bit is 1 to select SEG port function 1: Select SEGMENT port mode; 0: Select IO port mode

LCD_IO_SEL_3 (21H) LCD_SEG16-23 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG16-23 port selection configuration register, the corresponding bit is 1 to select SEG port function 1: Select SEGMENT port mode;

		0: Select IO port mode

LCD_IO_SEL_4 (22H) LCD_SEG24-27 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEG27/COM7	SEG26/COM6	SEG25/COM5	SEG24/COM4
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	LCD_SEG24-27 port selection configuration register, reserved in non-sharing mode, shared mode COM4~COM7 is LCD_SEG24-27 1: Select SEG24~SEG27 port/COM4~COM7; 0: Select IO port mode.

COM_IO_SEL (23H) COML select configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	In LED matrix drive mode, 4*4 mode is not selected: COM port select configuration register, the corresponding bit is 1, COMLx is common 1: Select the COM port function. 0: Select the I/O port mode In LED matrix drive mode, select 4*4 mode: COML0~ COML3 is common, and COML4~ COML7 is segment 1: Select COM port function or SEG port function; 0: Select the I/O port mode When the high current IO port drive is enabled: 1: Select the high-current I/O port 0: Select the I/O port mode

SEG_IO_SEL (24H) LED_SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LED_SEG0-7 port selection configuration register, the

		corresponding bit is 1, select SEG function 1: Select SEGMENT port mode; 0: Select IO port mode Note: This register is only valid when the LED matrix is not 4*4 mode.

DRAIN_EN (25H) PC4/5/PE4/5 port open drain output enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	--	PE5 port open drain output enable register 1: Open drain output 0: CMOS output
2	--	PE4 port open drain output enable register 1: Open drain output 0: CMOS output
1	--	PC5 port open drain output enable register 1: Open drain output 0: CMOS output
0	--	PC4 port open drain output enable register 1: Open drain output 0: CMOS output

ADC_IO_SEL0 (2AH) ADC function selection register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADC_IO_SEL0 [6:0]						
R/W	-	R/W						
Reset value	-	0						

Bit number	Bit symbol	Description
6~0	ADC_IO_SEL0[6:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 0000001=ADC0; 0000010=ADC1; 0000100=ADC2; 0001000=ADC3; 0010000=ADC4; 0100000=ADC5; 1000000=ADC6

SEL_LVDT_VTH (2CH) LVDT threshold selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	-	-	-	SEL_LVDT_VTH		
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	SEL_LVDT_VTH	LVDT threshold selection, the corresponding threshold is shown in the table "Threshold and Delay Selection" 000=2.7V; 001=3.0V; 010=3.8V; 011=4.2V; 100=3.3V; 101=3.6V; 110=4.0V; 111=4.4V

PD_ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	-	PD_LVDT	-	PD_XTAL_32K	-	PD_ADC
R/W	-	R/W	-	R/W	-	R/W
Reset value	-	1	-	1	-	1

Bit number	Bit symbol	Description
6	PD_LVDT	LVDT control register 1: Closed, 0: Open, closed by default
4	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz) control register, 1: Closed, 0: Open, closed by default
5, 3~1	--	Reserved
0	PD_ADC	Analog ADC shutdown control register: 0: ADC module works normally; 1: ADC module does not work

IDLE_WAKE_CFG (30H) System wakeup configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	PLL_WAKE_TIM		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	1	1	1

Bit number	Bit symbol	Description
2~0	PLL_WAKE_TIM	When PCON=1, wake up PLL timing time 000: 0.2ms; 001: 0.3ms;

		010: 0.4ms; 011: 0.5ms; 100: 0.6ms; 101: 0.7ms; 110: 0.9ms; 111: 1ms

LED_DRIVE (31H) LED port drive capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	LED port drive capability configuration register 0~15-4mA~78mA, Please refer to LED drive ammeter for details.

ADC_CFG_SEL (32H) ADC configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADCWNUM					ADC_I_SEL	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6~2	ADCWNUM	Selection of distance conversion interval time after sampling: (3+ADCWNUM)*T_{ADCK}
1	ADC_I_SEL[1]	ADC select comparator bias current 1: 4uA; 0: 5uA
0	ADC_I_SEL[0]	ADC select buffer bias current 1: 4uA; 0: 5uA

PWM_IO_SEL (33H) PWM port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	PWM_IO_SEL[7]	PWM3 port selection enable 1: Select PWM3 function; 0: Not select PWM3 function
6	PWM_IO_SEL[6]	PWM2 port selection enable

		1: Select PWM2 function; 0: Not select PWM2 function
5	PWM_IO_SEL[5]	PWM1C port selection enable 1: Select PWM1C function; 0: Not select PWM1C function
4	PWM_IO_SEL[4]	PWM1B port selection enable 1: Select PWM1B function; 0: Not select PWM1B function
3	PWM_IO_SEL[3]	PWM1A port selection enable 1: Select PWM1A function; 0: Not select PWM1A function
2	PWM_IO_SEL[2]	PWM0C port selection enable 1: Select PWM0C function; 0: Not select PWM0C function
1	PWM_IO_SEL[1]	PWM0B port selection enable 1: Select PWM0B function; 0: Not select PWM0B function. When PWM0B and PWM1D are configured at the same time, PWM0B is valid and PWM1D is invalid
0	PWM_IO_SEL[0]	PWM0A port selection enable 1: Select PWM0A function; 0: Not select PWM0A function. When PWM0A and PWM1E are configured at the same time, PWM0A is valid, and PWM1E is invalid

PERIPH_IO_SEL1 (34H) External port function selection register 1

Bit number	7	6	5	4
Symbol	UART1_IO_SEL	UART0_IO_SEL		IIC_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1
Bit number	3	2	1	0
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INT0_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_IO_SEL	UART1 port selection enable 0: Select UART1 (RXD1B/TXD1B) function; 1: Select UART1 (RXD1A/TXD1A) function
6~5	UART0_IO_SEL	UART0 port selection enable 00: select UART0 (RXD0C/TXD0C) function;

		01: Select UART0 (RXD0A/TXD0A) function; 1x: select UART0 (RXD0B/TXD0B) function
4	IIC_IO_SEL	IIC port selection enable 0: Select IIC (SCL0B/SDA0B) function; 1: Select IIC (SCL0A/SDA0A) function
3	INT3_IO_SEL	INT3 port selection enable 1: Select INT3 function; 0: Not select INT3 function
2	INT2_IO_SEL	INT2 port selection enable 1: Select INT2 function; 0: Not select INT2 function
1	INT1_IO_SEL	INT1 port selection enable 1: Select INT1 function; 0: Not select INT1 function
0	INT0_8_IO_SEL	INT0_8 port selection enable 1: Select INT function; 0: Not select INT function

PERIPH_IO_SEL2 (35H) External port function selection register 2

Bit number	7	6	5	4
Symbol	INT0_7_IO_SEL	INT0_6_IO_SEL	INT0_5_IO_SEL	INT0_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT0_3_IO_SEL	INT0_2_IO_SEL	INT0_1_IO_SEL	INT0_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT0_x_IO_SEL (x=7~0)	INT0_x port selection enable 1: Select INT function 0: Not select INT function

PERIPH_IO_SEL3 (36H) External port function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	INT4_7_IO_SEL	-	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-	-
Reset value	0	-	-	-	-	-	-	-

Bit number	Bit symbol	Description
7	INT4_7_IO_SEL	INT4_7 port selection enable 1: Select INT function; 0: Not select INT function
6~0	--	Reserved

PERIPH_IO_SEL4 (37H) External port function selection register 4

Bit number	7	6~3	2	1	0
Symbol	INT4_15_IO_SEL	-	INT4_10_IO_SEL	INT4_9_IO_SEL	INT4_8_IO_SEL
R/W	R/W	-	R/W	R/W	R/W
Reset value	0	-	0	0	0

Bit number	Bit symbol	Description
7, 2~0	INT4_x_IO_SEL (x=15, 10~8)	INT4_x port selection enable 1: Select INT function 0: Not select INT function
6~3	--	Reserved

PERIPH_IO_SEL5 (38H) External port function selection register 5

Bit number	7	6	5	4
Symbol	-	INT4_22_IO_SEL	INT4_21_IO_SEL	INT4_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	INT4_19_IO_SEL	INT4_18_IO_SEL	INT4_17_IO_SEL	INT4_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	--	Reserved
6~0	INT4_x_IO_SEL (x=22~16)	INT4_x port selection enable 1: Select INT function 0: Not select INT function

EXT_INT_CON1 (39H) External Interrupt configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	INT3_POLARITY		INT2_POLARITY		INT1_POLARITY		INT08_POLARITY	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1	0	1	0	1

Bit number	Bit symbol	Description
7~6	INT3_POLARITY	External interrupt 3 trigger polarity selection: 01: Falling edge (low level wake-up in Sleep mode) 10: rising edge (high level wake up in Sleep mode) 00/11: Double edge (low level wake up in Sleep mode)
5~4	INT2_POLARITY	External interrupt 2 trigger polarity selection: 01: Falling edge (low level wake-up in Sleep mode) 10: rising edge (high level wake up in Sleep mode) 00/11: Double edge (low level wake up in Sleep mode)

3~2	INT1_POLARITY	External interrupt 1 trigger polarity selection: 01: Falling edge (low level wake-up in Sleep mode) 10: rising edge (high level wake up in Sleep mode) 00/11: Double edge (low level wake up in Sleep mode)
1~0	INT08_POLARITY	External interrupt 0-8 trigger polarity selection: 01: Falling edge (low level wake-up in Sleep mode) 10: rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low level wake up in Sleep mode)

EXT_INT_CON2 (3AH) External Interrupt configuration register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	INT4_POLARITY	INT0_POLARITY	
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
2	INT4_ POLARITY	External Interrupt4_x trigger polarity selection: 1: Rising edge (high level wake-up in Sleep mode) 0: Falling edge (low-level wake-up in Sleep mode)
1~0	INT0_ POLARITY	External Interrupt0_0~0_7 trigger polarity selection: 01: Falling edge (low level wake-up in Sleep mode) 10: rising edge (high level wake up in Sleep mode) 00/11: Double edge (low level wake up in Sleep mode)

SPI_TX_START_ADDR (3EH) SPI high speed mode transmit buffer first address

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In SPI high-speed mode, the first address of the transmit data buffer, SPI_TX_START_ADDR*16

SPI_RX_START_ADDR (3FH) SPI high-speed mode receive cache header Address

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In SPI high-speed mode, the first address of the receive data buffer, SPI_RX_START_ADDR*16

SPI_NUM_L (40H) SPI high speed mode data cache address number low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPI_NUM_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPI_NUM_L[7:0]	SPI high speed mode data cache address number low 8 bits

SPI_NUM_H (41H) SPI high speed mode data cache address number high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SPI_NUM_H [3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	SPI_NUM_H[3:0]	SPI high speed mode data cache address number high 4 bits

ADC_CFG_SEL1 (42H) ADC comparator offset cancellation selection register

Bit number	7	6	5	4
Symbol	-	-	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	VREF_IN_ADC_SEL		CTRL_SEL	
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	0

Bit number	Bit symbol	Description
5	ADC_VREF_SEL	ADC reference voltage selection: 0: Select VCC as the output signal; 1: Select the voltage output by the ADC_VREF module as the reference voltage.
4	ADC_VREF_VOL_SEL	ADC_VREF output mode selection: 0: 2V as ADC reference voltage; 1: 4V as ADC reference voltage. When ADC_VREF output mode selects 2V/4V, it is recommended to select 3MHz for ADC frequency division clock
3~2	VREF_IN_ADC_SEL	Voltage selection input to the internal ADC channel of the chip 00: 1.362V; 01: 2.253V;

		10: 3.111V; 11: 4.082V;
1~0	CTRL_SEL	ADC offset elimination timing selection, the default value is 10: 00/01: first offset elimination and then sampling; 10/11: offset elimination and sampling are performed at the same time, 10 first-stage comparator switches are turned off at the end; 11: all switches are turned off at the same time open;

IIC_FIL_MODE (50H) IIC filter selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	IIC_AFIL_SEL	IIC_DFIL_SEL
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	0

Bit number	Bit symbol	Description
1	IIC_AFIL_SEL	IIC port analog filter selection enable 1: Select analog filter function; 0: Not select analog filter function.
0	IIC_DFIL_SEL	IIC port digital filter selection enable 1: Select digital filter function; 0: Not select digital filter function.

ADC_IO_SEL1 (53H) ADC select enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC7; 00000010=ADC8 00000100=ADC9; 00001000=ADC10; 00010000=ADC11; 00100000=ADC12; 01000000=ADC13; 10000000=ADC14

ADC_IO_SEL2 (54H) ADC select enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2 [7:0]							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC15; 00000010=ADC16 00000100=ADC17; 00001000=ADC18; 00010000=ADC19; 00100000=ADC20; 01000000=ADC21; 10000000=ADC22

ADC_IO_SEL3 (55H) ADC select enable register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC23; 00000010=ADC24 00000100=ADC25; 00001000=ADC26; 00010000=ADC27; 00100000=ADC28; 01000000=ADC29; 10000000=ADC30

ADC_IO_SEL4 (56H) ADC select enable register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL4 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL4 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC31; 00000010=ADC32; 00000100=ADC33; 00001000=ADC34; 00010000=ADC35; 00100000=ADC36;

		01000000=ADC37; 10000000=ADC38

ADC_IO_SEL5 (57H) ADC select enable register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	ADC_IO_SEL5 [4:0]				
R/W	-	-	-	R/W				
Reset value	-	-	-	0				

Bit number	Bit symbol	Description
7~5	--	Reserved
4~0	ADC_IO_SEL5 [4:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00001=ADC39; 00010=ADC40; 00100=ADC41; 01000=ADC42; 10000=ADC43;

LED_IO_START(58H) LED scan start selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	--	LED port serial dot matrix start PAD selection (only for LED serial dot matrix scan, and DUTY_SEL[2] needs to be configured to 0) 000: PB0 port; 001: PB1 port; 010: PB2 port; 011: PB3 port; 100: PB4 port; 101: PB5 port; 110: PB6 port; 111: PB7 port; See the table "LED dot matrix drive LEDX arrangement order"

PWM_IO_SEL1 (59H) PWM port selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W

Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PWM_IO_SEL[3]	PWM1E selection enable 1: PWM1E function is selected; 0: PWM1E function is not selected When PWM1E and PWM0_A are configured at the same time, PWM0A is valid and PWM1E is invalid
2	PWM_IO_SEL[2]	PWM1D selection enable 1: PWM1D function is selected; 0: PWM1D function is not selected. When PWM1D and PWM0_B are configured at the same time, PWM0B is valid and PWM1D is invalid
1	PWM_IO_SEL[1]	PWM0E selection enable 1: PWM0E function is selected; 0: PWM0E function is not selected
0	PWM_IO_SEL[0]	PWM0D selection enable 1: PWM0D function is selected; 0: PWM0D function is not selected

FLASH_BOOT_EN (5AH) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	FLASH_BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	FLASH_BOOT_EN	1: Indicates that the Flash BOOT upgrade mode has been entered, 0: Indicates that the Flash BOOT upgrade mode has been exited. Note: In Flash BOOT upgrade mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as BOOT upgrade function. {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses from 0x0000 to 0xFFFF.

EEP_SELECT (5BH) DATA area selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	1: Select NVR3 and NVR4 as DATA area When SPROG_ADDR_H[2]=1, select NVR4; When SPROG_ADDR_H[2]=0, select NVR3 0: Select address (0xFC00~0xFFFF) as DATA area, 1 page

PWM0_POLA_SEL (60H) PWM0 polarity selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
7~5	--	Reserved
4	--	PWM0E output polarity selection 1: Reverse output; 0: Normal output
3	--	PWM0D output polarity selection 1: Reverse output; 0: Normal output
2	--	PWM0C output polarity selection 1: Reverse output; 0: Normal output
1	--	PWM0B output polarity selection 1: Reverse output; 0: Normal output
0	--	PWM0A output polarity selection 1: Reverse output; 0: Normal output

PWM1_POLA_SEL (61H) PWM1 polarity selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
4	--	PWM1E output polarity selection 1: Reverse output; 0: Normal output
3	--	PWM1D output polarity selection 1: Reverse output; 0: Normal output
2	--	PWM1C output polarity selection 1: Reverse output; 0: Normal output
1	--	PWM1B output polarity selection 1: Reverse output; 0: Normal output

0	--	PWM1A output polarity selection 1: Reverse output; 0: Normal output

XTAL_CLK_SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	Crystal frequency selection register 1: Select 4MHz; 0: Select 32768Hz

SEL_LVDT_DELAY (65H) LVDT delay control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	SEL_LVDT_DELAY	Select signal, select LVDT power-down delay 00: Delay time 1; 01: Delay time 2; 10: Delay time 3; 11: Delay time 4

BOR_SEL (66H) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEL_BOR_DELAY	SEL_BOR_VTH		
R/W	-	-	-	-	R/W	R/W		
Reset value	-	-	-	-	0	0		

Bit number	Bit symbol	Description
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2
2~0	SEL_BOR_VTH	BOR threshold selection 00x: 2.3V; 010: 2.8V; 011: 3.3V; 100: 3.7V; 1xx: 4.2V;

UART_BD_EXT (67H) UART0/1/2 baud rate configuration extension bit register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	UART0/1/2 baud rate configuration extension bit selection 1: Select the baud rate to extend to 12 bits; 0: Select the baud rate without extension to maintain 10 bits

SPI_IO_SEL (68H) SPI communication port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	SPI_IO_SEL[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	SPI_IO_SEL[1:0]	SPI communication port selection register 01: PC2/3/4/5 selects SPI function 10: PE4/5/6/7 selects SPI function 00/11: PG0/1/2/3 selects SPI function

SPI_MCLK_MOD (69H) SPI master mode receiver clock selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	SPI master mode receiver clock selection register 1: Select the host output as the receive clock; 0: Select the PAD port input as the receive clock

BOOT_CMD (6AH) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Configure the program space jump instruction, write 5 groups of data continuously (0xFF, 0x00, 0x88, 0x55, 0xAA), jump into the main program space; write 5 groups of data continuously (0x37, 0xC8, 0x42, 0x9A, 0x65), Jump into the Boot program space; the value read out is the byte written recently.

ROM_OFFSET_L (6BH) Address offset of CODE area, low 8 bits

Bit number	7	6	5	4	3	2	1	0

Symbol	-
R/W	R
Reset value	0

Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (low 8 bits)

ROM_OFFSET_H (6CH) Address offset of CODE area, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Address offset of CODE area (high 8 bits)

Note:

1. **’-’: Reserved;**
2. **The reserved register and the reserved bit of the register are forbidden to write, otherwise it may cause the chip to be abnormal.**

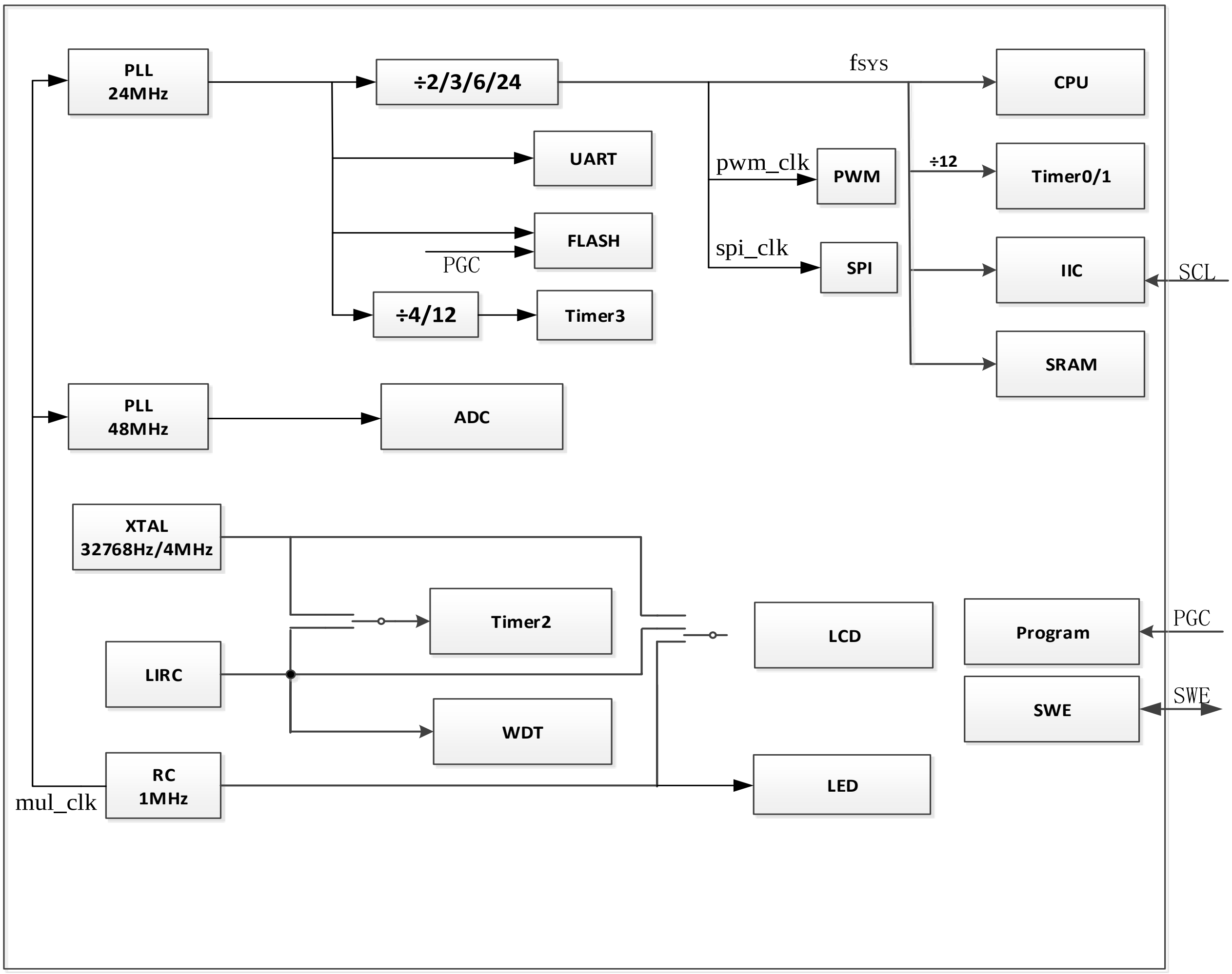
5. Clock, Reset, Working Mode and Watchdog

5.1. Clock

5.1.1. Introduction

Clock source:

- Internal high-speed RC oscillator: RC1M
- Internal low-speed RC oscillator: LIRC32k
- External crystal oscillator: 32768 Hz/4 MHz
- RC1M multiplication to get PLL clock: PLL48M/ PLL24M



Clock block diagram

The BF7515CM44-LJTX series clock is defined as follows:

RC1MHz: Built-in RC oscillator, RC1MHz is used as LCD/LED Driver clock.

PLL_24MHz: The 24MHz clock generated by the phase-locked loop is used as the main system clock after frequency division.

f_{SYS}: PLL_24MHz clock divided by frequency, the frequency is 12MHz/8MHz/4MHz/1MHz.

pwm_clk: PWM working clock, frequency 12MHz/8MHz /4MHz/1MHz optional.
spi_clk: SPI working clock, frequency 12MHz/8MHz /4MHz/1MHz optional.
PLL_48MHz: The 48MHz clock generated by the phase-locked loop is used as the clock source of ADC.
XTAL32768Hz/4MHz: External precision clock, can be used as Timer2 or LCD Driver clock.
LIRC: The internal low-speed clock is 32 kHz, which is used as watchdog clock, Timer2 clock or LCD Driver clock.
SCL: The frequency is 100 kHz/400 kHz, as the IIC communication clock.
PGC: Flash programming clock, frequency range 100 kHz~5MHz, download clock when programming and burning programs.

5.1.2 Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0xAD	SYS_CLK_CFG	RW	xxx0_1000b	System clock configuration register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register
0x30	IDLE_WAKE_CFG	RW	xxxx_x111b	System wake-up configuration register
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register

SYS_CLK_CFG (ADH) System clock configuration register

Bit number	7~5	4	3	2	1	0
Symbol	-	IM0_EN	PLL_CLK_SEL			PD_SYS_CLK
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	1	0	0	0

Bit number	Bit symbol	Description
7~5	--	Reserved
3~1	PLL_CLK_SEL	PLL clock divider selection register: 000/100: 12MHz; 001/101: 8MHz; 010/110: 4MHz; 011/111: 1MHz
0	PD_SYS_CLK	Core clock enable 0: Turn on core working clock; 1: Turn off core working clock

TIMER2_CFG (93H) TIMER2 configuration register

Bit number	7~4	3	2	1	0
Symbol	-	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
2	TIMER2_CLK_SEL	Timer2 clock select register 1: Select XTAL32768Hz/4MHz; 0: Select LIRC

TIMER3_CFG (84H) TIMER3 configuration register

Bit number	7~3	2	1	0
Symbol	-	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
2	TIMER3_CLK_SEL	TIMER3 timing clock selection register 1: Select clk_24M/4; 0: Select clk_24M/12

Secondary bus register:

PD_ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	-	PD_LVDT	-	PD_XTAL_32K	-	PD_ADC
R/W	-	R/W	-	R/W	-	R/W
Reset value	-	1	-	1	-	1

Bit number	Bit symbol	Description
4	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz/4MHz) control register 1: Off; 0: On, default off

XTAL_CLK_SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	Crystal frequency selection register

		1: Select 4MHz; 0: Select 32768Hz

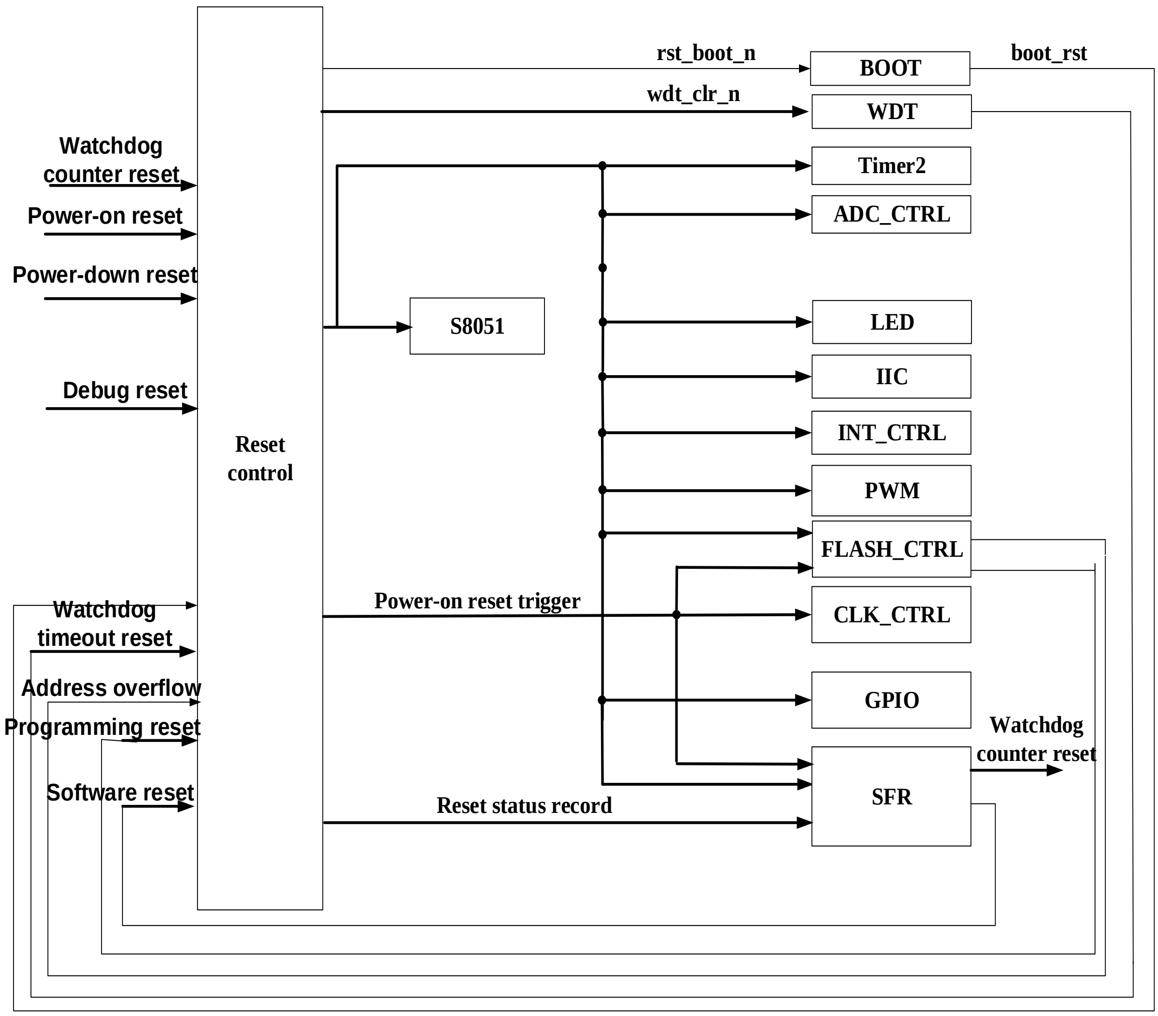
IDLE_WAKE_CFG (30H) System wake-up configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	PLL_WAKE_TIM		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	1	1	1

Bit number	Bit symbol	Description
2~0	PLL_WAKE_TIM	When PCON=1, wake-up PLL timing time 000: 0.2ms; 001: 0.3ms; 010: 0.4ms; 011: 0.5ms; 100: 0.6ms; 101: 0.7ms; 110: 0.9ms; 111: 1ms

5.2. Reset System

There are eight reset modes in the BF7515CM44-LJTX: power-on reset, power-off reset, programming reset, software reset, modify configuration reset, watchdog timer overflow reset, PC pointer overflow reset, ROM address jump reset. Any one of above reset, global will make chip reset. We can judge the reset flag register which reset happen, the reset must be cleared by software.



Reset block diagram

5.2.1. Reset Sequence

po_n: Power-on reset. After the system is powered on, the analog module generates a low-level signal and lasts for 93ms. When the power-on reset is low, the entire chip is in the reset state, and after the global reset signal continues to be effective 20ms after the power-on reset is high, the system exits the reset mode.

bo_n: brown-out reset. The analog module generates a low-level signal after the system has a power-down reset. When the power-down reset signal is low, the entire chip is in the reset state. After the global reset signal becomes high, the system exits the reset mode after the global reset signal continues to be valid for 20ms.

soft_rst: software reset. The soft reset signal is valid by writing SFR, and the global reset signal is valid for 20ms. After 20ms, the system exits the reset mode.

prog_en: programming reset. When prog_en is high, it is the programming mode of FLASH. At this time, the global reset signal is valid. After it goes low, the global reset signal continues to be valid for 20ms.

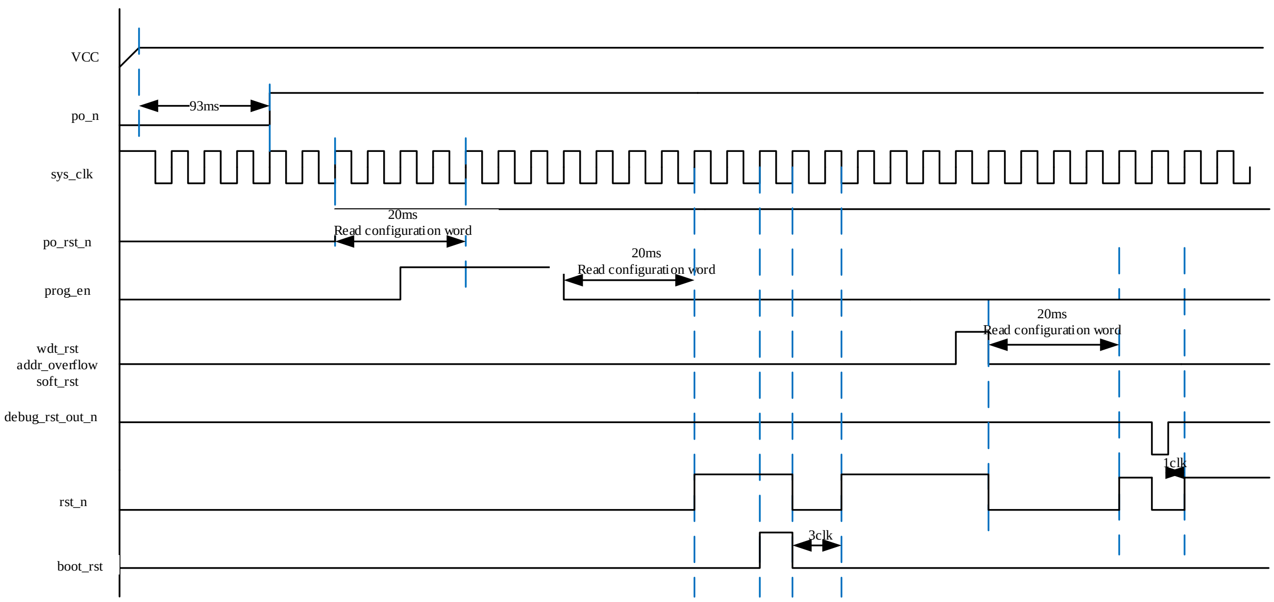
wdt_rst: The watchdog timer overflow reset. After the watchdog timer overflows, the global reset is 20ms. After 20ms, the system exits the reset mode.

addr_overflow: PC pointer overflow reset. If the PC pointer exceeds the valid address range of the flash when the MCU addresses the program memory, the addr_overflow signal becomes high, and the sys_clk clock rising edge detects the high level of addr_overflow (requires 1 clock cycle) and resets the global 20ms, the reset signal will clear the addr_overflow signal to zero. After 20ms, the system exits the reset mode.

debug_rst_out_n: trim configuration reset, output a reset signal for the core trim module, low means reset is effective, chip global reset, but there will not be a 20ms initialization process, only delay 1 system clock reset low level.

boot_rst: ROM Address jump reset, the boot_rst signal becomes high after the complete ROM space jump instruction is configured, and the sys_clk clock checks the boot_rst high level (valid for one clock cycle) to reset the global, but there will be no 20ms read configuration word process. Only delay the reset low level of 3 System clocks.

Reset sequence description:

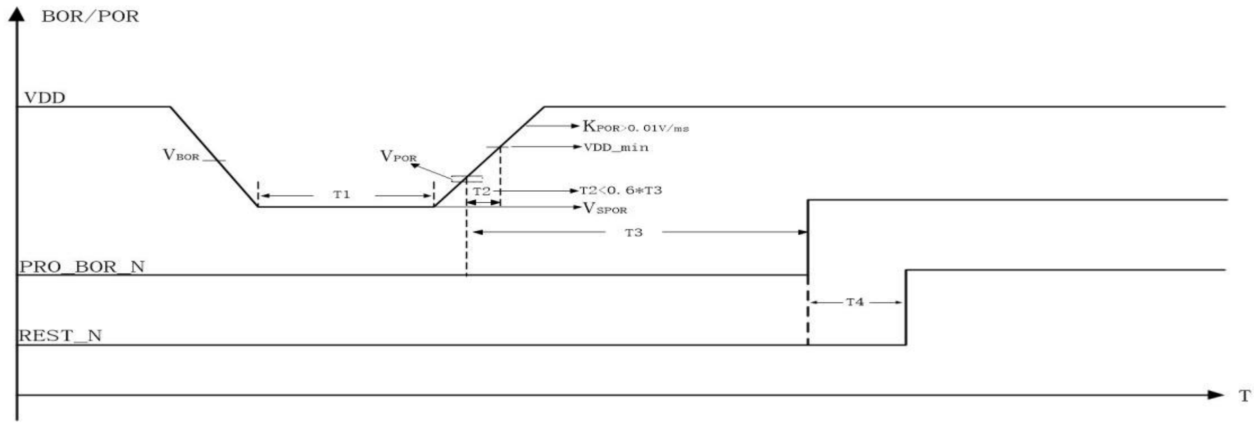


1. The chip has a power-on reset, and the analog POR module delays for 93ms, and po_n is pulled high.
2. The programmer sends instructions to make the chip enter the programming mode (prog_en is pulled high). In the programming mode, the system is in a global reset state. After the

programming is completed, the programming mode is exited. After a delay of 20ms, rst_n is pulled high and the chip enters normal operation.

3. During normal operation, any one of watchdog reset, address overflow reset, soft reset, ROM address jump reset occurs, rst_n is pulled low, after a delay of 20ms, rst_n is pulled high, and the chip enters normal operation.
4. After normal work, you cannot enter the programming mode.
5. In debug mode, configure debug reset, pull down rst_n, pull up 1 system clock in debug_rst_out_n, pull up rst_n, and the chip enters normal operation.
6. When the chip supports the BOOT upgrade function, a ROM Address jump reset occurs, rst_n is pulled low, after 3 System clocks, rst_n is pulled high, and the chip enters normal operation.

BOR / POR Chart:



BOR/POR chart diagram

BOR/POR reset parameters:

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VCC	temperature				
V_{SPOR}	Power on reset start voltage	-	25℃	-	-	300	mV
K_{POR}	Power on reset voltage rate	-	25℃	0.01	-	-	V/ms
V_{POR}	Power on reset voltage	-	25℃	1.1	1.5	2.2	V
V_{BOR}	Brownout reset voltage (±10%), hysteresis 0.2V	-	25℃	-	V_{BOR}	-	V
VDD_min	Minimum operating voltage	-	25℃	2.7	-	-	V
T1	VDD keep VSPOR time	-	25℃	0.1	-	-	ms
T2	VPOR from VDD_min time	-	25℃	-	-	0.6*T3	ms
T3	Reset POR_BOR_N duration	-	25℃	55	93	131	ms
T4	Global reset effective time	-	25℃	-	20	-	ms

Power on reset parameter characteristic table

Note: VBOR power-down reset voltage is selected by register BOR_SEL [2:0].

When VDD is affected by the load or severely disturbed, if the voltage drops into the voltage dead zone and the chip is not within the working voltage range, it may cause the system to work abnormally. The function of power-down reset (BOR) is to monitor when VDD drops to the BOR voltage, the MCU can generate a power-down reset in advance to avoid system errors.

Suggestions to prevent entering the voltage dead zone and reduce the probability of system error:

- Increase the voltage drop slope

5.2.2. Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x8E	SOFT_RST	RW	0000_0000b	Soft reset register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x0F	RST_STAT	RW	0000_0010b②	Reset flag register
0x66	BOR_SEL	RW	xxxx_0000b③	BOR control register

②: The power-on reset is 1. Other resets: Reset to 0 after power-on and 1 after corresponding reset.

③: The register is reset after power-on. Other resets do not change the configuration value.

SOFT_RST (8EH) Soft reset register

Bit number	7	6	5	4	3	2	1	0
Symbol	SOFT_RST[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SOFT_RST[7:0]	Soft reset register, only when the register value is 0x55, the software reset is generated

Secondary Bus Register:

BOR_SEL (66H) BOR control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEL_BOR_DELAY	SEL_BOR_VTH		
R/W	-	-	-	-	R/W	R/W		
Reset value	-	-	-	-	0	0		

Bit number	Bit symbol	Description
3	SEL_BOR_DELAY	Select the signal, select the power-down delay of BOR 0: Delay time 1; 1: Delay time 2
2~0	SEL_BOR_VTH	BOR threshold selection 00x: 2.3V; 010: 2.8V; 011: 3.3V; 100: 3.7V; 1xx: 4.2V;

SEL_BOR_DELAY	SEL_BOR_VTH	BOR			
		Power down	Recovery	Hysteresis	Delay

		threshold (V)	threshold (V)	(mV)	(µs)
0	000	2.3	2.4	143	68.1
	001	2.3	2.4	143	68.1
	010	2.8	2.9	140	84.5
	011	3.3	3.4	145	98.3
	100	3.7	3.8	120	108
	101/110/111	4.2	4.3	130	118.1
1	000	2.3	2.4	146	135.2
	001	2.3	2.4	146	135.2
	010	2.8	2.9	144	168.5
	011	3.3	3.4	150	196.5
	100	3.7	3.8	127	216
	101/110/111	4.2	4.3	135	236.3

RST_STAT (0FH) Reset flag register

Bit number	7	6	5	4	3	2	1	0
Symbol	BOOT_ F	DEBUG_ F	SOFT_ F	PROG_ F	ADD ROF_F	BO_F	PO_F	WDT RST_F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	1	0

Bit number	Bit symbol	Description
7	BOOT_F	0: No effect; 1: A reset occurs when the configuration program space jumps.
6	DEBUG_F	0: No effect; 1: trim configuration reset occurred.
5	SOFT_F	0: No effect; 1: software reset occurred.
4	PROG_F	0: No effect; 1: program reset occurred.
3	ADDROF_F	0: No effect; 1: PC pointer overflow reset occurred.
2	BO_F	0: No effect; 1: Power_down reset occurred.
1	PO_F	0: No effect; 1: Power_on reset occurred.
0	WDTRST_F	0: No effect; 1: watchdog timer overflow reset occurred.

5.3. Working Mode

5.3.1. Introduction

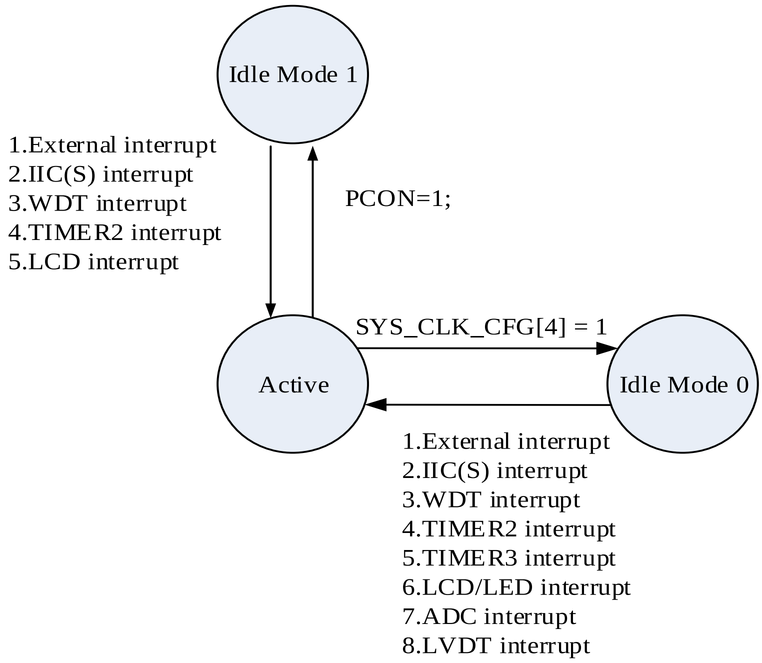
BF7515CM44-LJTX series working mode: active mode, standby mode.

BF7515CM44-LJTX provides SYS_CLK_CFG register, configure Bit4 of this register to control MCU to enter idle mode 0. BF7515CM44-LJTX provides PCON register, configure Bit0 of this register to control MCU to enter idle mode 1.

- **Active Mode**
  RC1M, PLL, LIRC work, XTAL depends on software configuration. The core runs, the peripherals keep working normally, and the functions of each peripheral are controlled by software configuration.
- **Standby mode is divided into idle mode 0 and idle mode 1**
  - **Idle Mode 0**
    RC1M, PLL, LIRC work, XTAL depends on software configuration. The core stops running, the UART, PWM, SPI peripherals do not work, and the rest of the peripherals can work.
  - **Idle Mode 1**
    RC1M and PLL are off, LIRC works, XTAL depends on software configuration. The core is stopped and the peripherals work fine using the LIRC clock.

Mode	Conditions	Effect on clock results	
Active Mode	Wake-up from power-on reset/standby mode	RC1M	Work
		PLL	Work
		LIRC	Work
		XTAL32K/4M	Depends on software configuration
Idle Mode 0	SYS_CLK_CFG[4] =1	RC1M	Work
		PLL	Work
		LIRC	Work
		XTAL32K/4M	Depends on software configuration
Idle Mode 1	PCON=1	RC1M	Close
		PLL	Close
		LIRC	Work
		XTAL32K/4M	Depends on software configuration

The working state of the clock source in each mode



Working mode conversion diagram

5.3.2. Low power management

All CPU states are saved before entering standby mode, SRAM and register contents are preserved, and GPIOs remain in run-time state. In addition, all modules can be individually configured to close the gate, thereby reducing power consumption.

The working status of BF7515CM44-LJTX series is shown in the following table

NO	Module Name	Clock source	Active Mode	Idle Mode 0	Idle Mode 1
1	s8051	f_{SYS}	√	×	×
2	UART0~1	PLL_24M	○	×	×
3	PWM0~3	PLL_48M	○	×	×
4	Timer0	f_{SYS}	○	×	×
5	Timer1	f_{SYS}	○	×	×
6	Timer2	LIRC/ XTAL	○	○	○
7	Timer3	PLL_24M	○	○	×
8	LED	RC1M	○	○	×
9	LCD	LIRC/XTAL/RC1M	○	○	○
10	WDT	LIRC	○	○	○
11	ADC_CTRL	PLL_48M	○	○	×
12	IIC(S)	f_{SYS}	○	○	○
13	SPI	PLL_48M	○	○	×

Note: '○': According Configuration

Ways to exit the Idle Mode 0:

Enabling any one of IIC, External Interrupt0/1/2/3/4, WDT, Timer3, Timer2, LCD, LED, ADC, LVDT to wake up the chip; Exit the Idle Mode 0, and the CPU executes the interrupt service routine.

Ways to exit Low_power mode:

Enabling IIC, External Interrupt0/1/2/3/4, WDT, Timer2, LCD interrupt generation can wake up the chip; Exit Low_power mode, after the interrupt response is generated. The CPU executes the interrupt service program related to the interrupt vector, and returns to the next instruction after the execution of the RETI return instruction to make the CPU enter the Low_power mode to continue running the program.

5.3.3. Register

SYS_CLK_CFG (ADH) System clock configuration register

Bit number	7~5	4	3	2	1	0
Symbol	-	IM0_EN	PLL_CLK_SEL			PD_SYS_CLK
R/W	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	1	0	0	0

Bit number	Bit symbol	Description
4	IM0_EN	Idle Mode 0 enable 1: Enter Idle Mode 0; 0: Exit Idle Mode 0

PCON(87H) Idle mode 1 select register

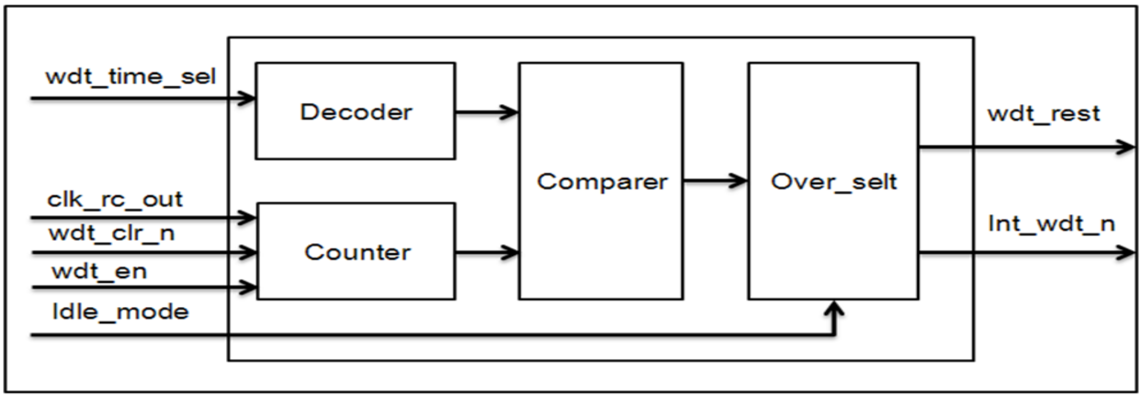
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	IM1_EN
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
7~1	--	Reserve
0	IM1_EN	Idle Mode 1 Enable 1: Idle mode 1; 0: Active mode, automatically cleared after wake-up Note: The software delay must be ≥100μs after wake-up, otherwise the wake-up function is abnormal

5.4. WDT

5.4.1. Introduction

The watchdog timer counting circuit uses the internal low-speed clock LIRC for timing, and the configurable timing time is 2^n*18ms (n=0, 1, 2, 3, 4, 5, 6, 7) ----- here n is the configuration value of the timing configuration register.



Due to the particularity of the system application, the watchdog timer overflow signal is classified:

In the normal working mode, if the watchdog timer overflow occurs, the overflow signal is the watchdog overflow reset signal at this time, and the watchdog overflow reset affects the global reset. At this time, the system realizes the global reset action and reloads the configuration information;

In the idle mode 1, if a watchdog timer overflow occurs, the overflow signal is the watchdog interrupt signal at this time, and the interrupt wakes up the chip to exit the idle mode 1 and execute the watchdog interrupt service function.

The watchdog module is a timing counting module. Its count clock is the internal low-speed clock LIRC. Its timing clear signal is composed of global reset and configuration clear. This signal is synchronously released by the watchdog timing clock in the reset module; The clearing action is generated every time the CPU configures the watchdog timer configuration register (WDT_CTRL), and the watchdog restarts timing; at the same time, the watchdog counter has the watchdog count enable control, when the count enable is valid, After the watchdog generates a timing overflow (reset or interrupt), as long as the watchdog counting enable is not turned off, the watchdog counter will restart counting.

5.4.2. WDT Related Register

SFR register				
Address	Name	RW	Reset	Description
0x91	WDT_CTRL	RW	xxxx_x000b	Watchdog overflow timing configuration register

0x92	WDT_EN	RW	0000_0000b	WDT timing enable configuration register
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

WDT SFR register list

WDT_ CTRL (91H) Watchdog overflow timing configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WDT_TIME_SEL		
R/W	-	-	-	-	-	R/W		
Reset value	-	-	-	-	-	0		

Bit number	Bit symbol	Description
2~0	WDT_TIME_SEL	Watchdog overflow timing configuration register, the timing length is as follows: 0x00: 18ms; 0x01: 36ms; 0x02: 72ms; 0x03: 144ms; 0x04: 288ms; 0x05: 576ms; 0x06: 1152ms; 0x07: 2304ms;

The watchdog uses the internal low-speed clock LIRC to complete the timing function and can achieve timing from 18ms to 2.3s. The timing length is controlled by SFR (WDT_CTRL).

WDT_EN (92H) Watchdog timer enable configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	WDT_EN							
R/W	R/W							
Reset value	0							

Turn off WDT when writing 0x55, write other values to enable WDT, the WDT always works after the reset is over. Clearing the WDT is done by writing to the WDT_CTRL register. Whichever values is written to this register will clear the WDT.

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

4	INT_WDT_STAT	WDT interrupt status flag, this bit is cleared by writing 0 to zero, and it can also be cleared by writing WDT_CTRL. 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	EX5	EX4	EX3	EX2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value	0	0	0	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2/PWM0 interrupt enable 1: WDT/Timer2/PWM0 interrupt enable; 0: WDT/Timer2/PWM0 interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag 1: With interrupt flag; 0: Without interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit 1: WDT/Timer 2/PWM0 interrupt is high priority; 0: WDT/Timer 2/PWM0 interrupt is low priority

6. GPIO

Some pins of the GPIO port are multiplexed with device peripheral functions, and cannot be configured as multiple clock functions at the same time, otherwise it will cause malfunction. IIC communication port, open-drain output, pull-up resister required.

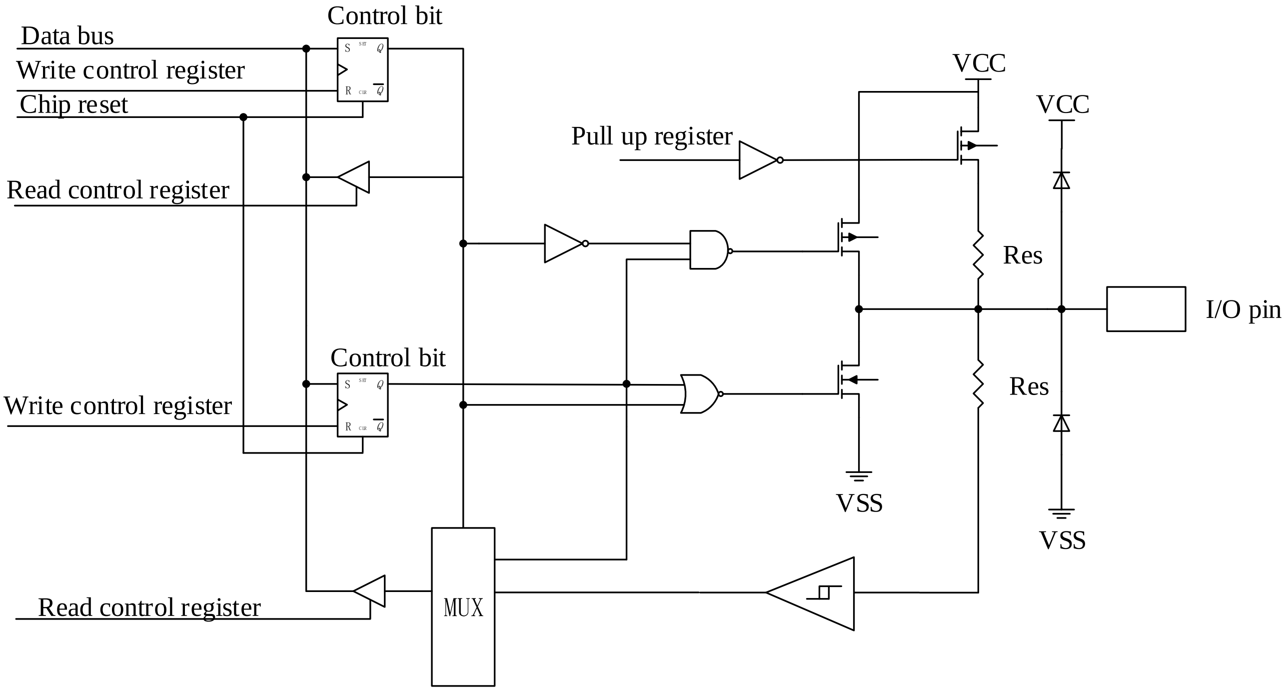
TRISX register (Direction Register): TRISX set to 1 can be configured as input pin, set to 0 can be configured as output pin.

DATAX register (Data Register): DATAX set to 1 the data in DATAX will be configured as high, set to 0 the data in DATAX will be configured as low.

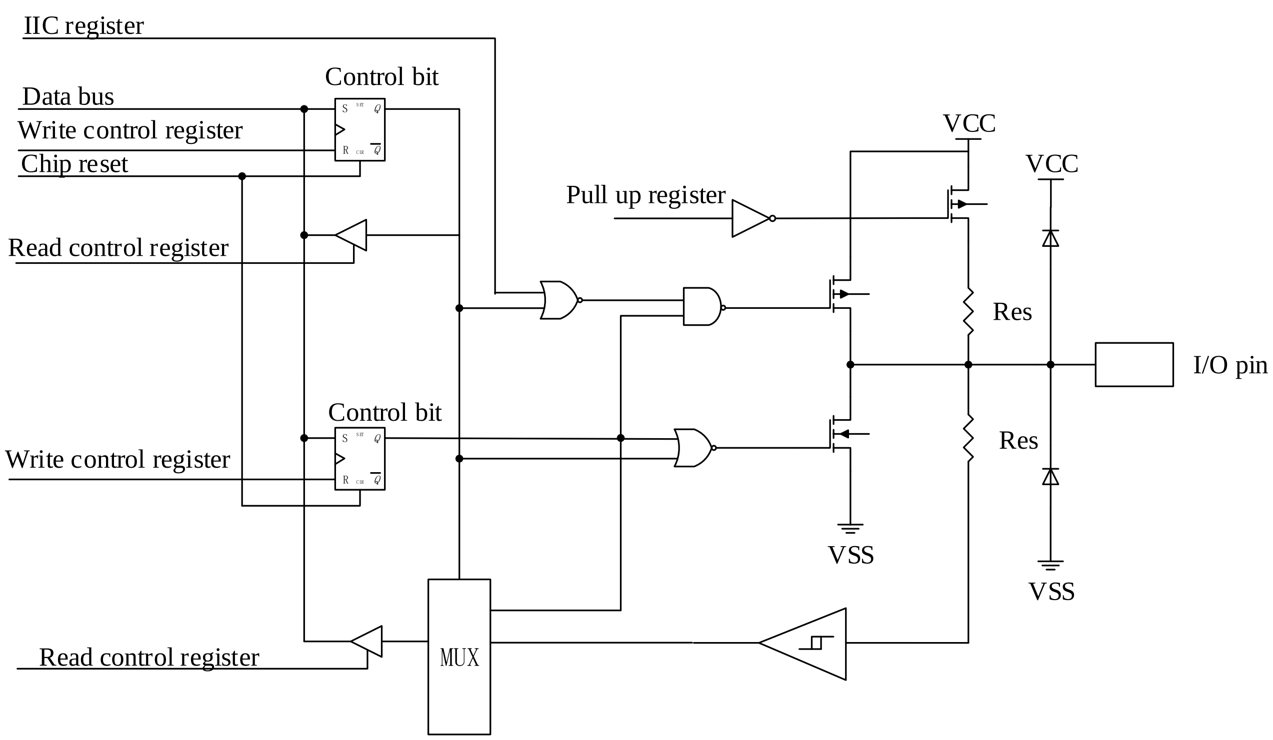
PU_PX register (pull-up resistor enable register): the pin corresponding to PU_PX is set to 1 is enabled, and the corresponding pin is cleared to disable the pull-up resistor, and the pull-up resistor is 35k.

ODRAIN_EN register: Set ODRAIN_EN to 1 to enable open-drain output on the corresponding pin. Clear it to disable open-drain output. After enabling IIC function, open-drain output is automatically turned on. IIC/UART recommends using external pull-up resistors.

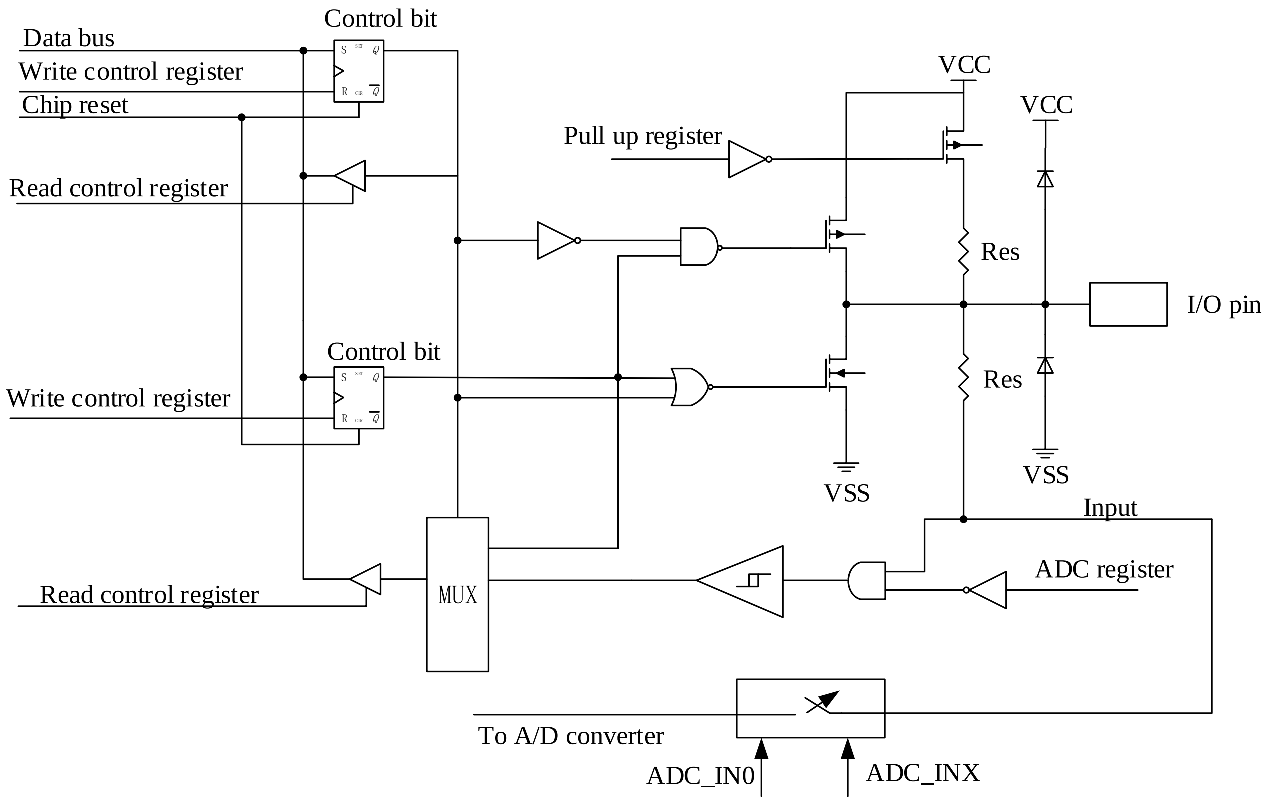
Supports high current drive function of 8 GPIO ports.



General IO structure



Open-drain output structure



ADC IO structure

6.1. GPIO Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x80	DATAB	RW	1111_1111b	PB port data register
0x90	DATAC	RW	1111_1111b	PC port data register
0xB0	DATAE	RW	1111_1111b	PE port data register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xC0	DATAF	RW	1111_1111b	PF port data register
0xC8	DATAG	RW	xxxx_1111b	PG port data register
0xD8	DATAH	RW	1111_1111b	PH port data register
0xEA	TRISA	RW	xxxx_1111b	PA direction register
0xEB	TRISB	RW	1111_1111b	PB direction register
0xEC	TRISC	RW	1111_1111b	PC direction register
0xEE	TRISE	RW	1111_1111b	PE direction register
0xEF	TRISF	RW	1111_1111b	PF direction register
0xF2	TRISG	RW	xxxx_1111b	PG direction register
0xF7	TRISH	RW	1111_1111b	PH direction register
0xF8	DATAA	RW	xxxx_1111b	PA port data register

Port configuration SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x17	PU_PA	RW	xxxx_0000b	PA pull-up resistor control register
0x18	PU_PB	RW	0000_0000b	PB pull-up resistor control register
0x19	PU_PC	RW	0000_0000b	PC pull-up resistor control register
0x1B	PU_PE	RW	0000_0000b	PE pull-up resistor control register
0x1C	PU_PF	RW	0000_0000b	PF pull-up resistor control register
0x1D	PU_PG	RW	xxxx_0000b	PG pull-up resistor control register
0x1E	PU_PH	RW	0000_0000b	PH pull-up resistor control register
0x23	COM_IO_SEL	RW	0000_0000b	COM selection configuration register
0x25	ODRAIN_EN	RW	xxxx_0000b	PC4/5/PE4/5 port open drain output enable register

Port configuration secondary bus register list

6.2. GPIO Register Description

6.2.1. Port Data Register

DATAA (F8H) PA port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PA3	PA2	PA1	PA0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	PA data register, you can configure the output level of the PA group IO port as GPIO port, the read value is the current level state of the IO port (input) or the configured output value (output)

DATAB (80H) PB port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PB data register, configurable PB group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAC (90H) PC port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PC data register, configurable PC group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAE (B0H) PE port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PE data register, configurable PE group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAF (C0H) PF port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PF data register, you can configure the output level of the PF group IO port as a GPIO port, and the read value is the current level state of the IO port (input) or the configured output value (output)

DATAG (C8H) PG port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PG3	PG2	PG1	PG0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	PG data register, configurable PG group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

DATAH (D8H) PH port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	PH data register, configurable PH group IO port as GPIO port output level, the read value is the current level state of IO port (input) or configured output value (output).

6.2.2. Direction Register

TRISA (EAH) PA direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	Bit[3]~ Bit[1]: Direction of PA3~PA0 port pins 0: PAx port is output; 1: PAx port is input

TRISB (EBH) PB direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: Direction of PB7~PB0 port pins 0: PBx port is output; 1: PBx port is input

TRISC (ECH) PC direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: Direction of PC7~PC0 port pins 0: PCx port is output; 1: PCx port is input

TRISE (EEH) PE direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: Direction of PE7~PE0 port pins

		0: PEx port is output; 1: PEx port is input

TRISF (EFH) PF direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: Direction of PF7~PF0 port pins 0: PFx port is output; 1: PFx port is input

TRISG (F2H) PG direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	1	1	1	1

Bit number	Bit symbol	Description
3~0	--	Bit[3]~ Bit[1]: Direction of PG3~PG0 port pins 0: PGx port is output; 1: PGx port is input

TRISH (F7H) PH direction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit number	Bit symbol	Description
7~0	--	Bit[7]~ Bit[1]: Direction of PH7~PH0 port pins 0: PHx port is output; 1: PHx port is input

6.2.3. Pull-up Enable Register

Secondary bus register:

PU_PA (17H) PA pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W

Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	PA pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PB (18H) PB pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PB pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PC (19H) PC pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PC pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PE (1BH) PE pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PE pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PF (1CH) PF pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							

Reset value	0

Bit number	Bit symbol	Description
7~0	--	PF pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PG (1DH) PG pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	PG pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

PU_PH (1EH) PH pull-up resistor control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	PH pull-up resistor control register 1: The pull-up resistor is enabled; 0: The pull-up resistor is not enabled

6.2.4. Large Current Sink

DP_CON (B1H) LCD, LED control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	IO_ON	DUTY_SEL			DPSEL	SCAN_MODE	COM_MOD
R/W	-	R/W	R/W			R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
0	COM_MOD	High-current IO port driver enable 1: COM port function is locked and works as a high-current IO port; 0: COM port function is not locked and can be configured as

		other functions; When COM port function is locked to high-current IO port, by configuring GPIO register output drive timing, LED/LCD scan configuration is invalid

COM_IO_SEL (23H) COML select configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	In LED matrix drive mode, 4*4 mode is not selected: COM port select configuration register, the corresponding bit is 1, COMLx is common 1: Select the COM port function. 0: Select the I/O port mode In LED matrix drive mode, select 4*4 mode: COML0~ COML3 is common, and COML4~ COML7 is segment 1: Select COM port function or SEG port function; 0: Select the I/O port mode When the high current IO port drive is enabled: 1: Select the high-current I/O port 0: Select the I/O port mode

6.2.5. Open Drain Enable Register

Secondary bus register:

DRAIN_EN (25H) PC4/5/PE4/5 port open drain output enable register

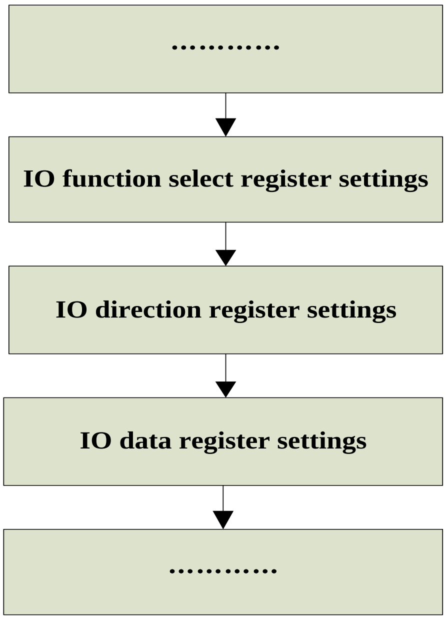
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	--	PE5 port open drain output enable register 1: Open-drain output; 0: CMOS output
2	--	PE4 port open drain output enable register 1: Open-drain output; 0: CMOS output
1	--	PC5 port open drain output enable register 1: Open-drain output; 0: CMOS output

0	--	PC4 port open drain output enable register 1: Open-drain output; 0: CMOS output

6.3. GPIO Configuration Process

When setting the port as GPIO, the following three sets of registers need to be set accordingly.



IO configuration flow chart

Note:

The default source current drive capability of the IO port is typically 16mA, and the sink current drive capability is typically 68mA @5V 0.9VCC. When using IO to drive the LED/digital tube, you need to pay attention to the Ifp current of the LED lamp. It is recommended to add a current-limiting resistor to limit the IO drive peak current within the LED/digital tube Ifp current.

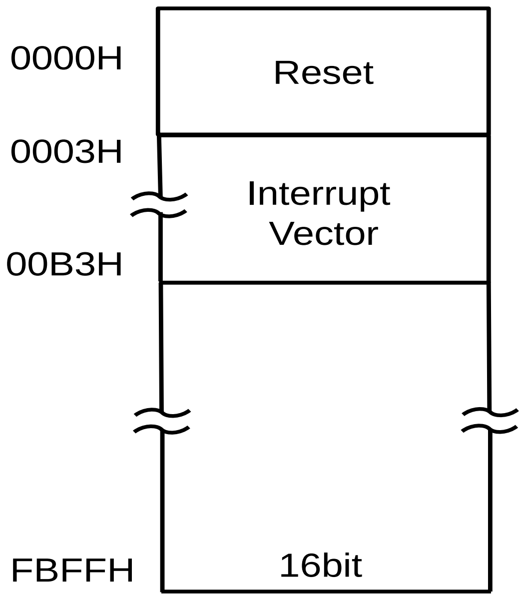
7. Interrupt

7.1. Interrupt Sources and Entry Address

Interrupt source	Condition	Sign	Enable control	Priority control	Interrupt vector	Query priority	Interrupt number	Flag removal method	wakeup idle mode 1
INT0	condition is met	IE0	IEN0[0]	IPL0[0]	0x0003	1	0	△	Yes
Timer0	Timer0 overflow	TF0	IEN0[1]	IPL0[1]	0x000B	2	1	△	No
INT1	condition is met	IE1	IEN0[2]	IPL0[2]	0x0013	3	2	△	Yes
Timer1	Timer1 overflow	TF1	IEN0[3]	IPL0[3]	0x001B	4	3	△	No
INT2	condition is met	IE2	IEN1[2]	IPL1[2]	0x004B	5	9	△	Yes
IIC	Receive or send completed	IE3	IEN1[3]	IPL1[3]	0x0053	6	10	△	Yes
ADC	ADC conversion completed	IE4	IEN1[4]	IPL1[4]	0x005B	7	11	△	No
LED/ LCD	Scan complete	IE6	IEN1[6]	IPL1[6]	0x006B	9	13	△	No
WDT/ Timer2 /PWM0	WDT/Timer2/ PWM0 overflow	IE7	IEN1[7]	IPL1[7]	0x0073	10	14	△	WDT/ Timer2 yes, PWM0 no
UART2	Receive or send completed	IE8	IEN2[0]	IPL2[0]	0x007B	11	15	△	No
LVDT	Voltage Conditions meet	IE9	IEN2[1]	IPL2[1]	0x0083	12	16	△	No
UART0	Receive or send completed	IE10	IEN2[2]	IPL2[2]	0x008B	13	17	△	No
UART1	Receive or send completed	IE11	IEN2[3]	IPL2[3]	0x0093	14	18	△	No
Timer3/PWM1	Timer3/PWM1 overflow	IE12	IEN2[4]	IPL2[4]	0x009B	15	19	△	No
SPI	Receive or send completed	IE13	IEN2[5]	IPL2[5]	0x00A3	16	20	△	No
INT3	condition is met	IE14	IEN2[6]	IPL2[6]	0x00AB	17	21	△	Yes
INT4	condition is met	IE15	IEN2[7]	IPL2[7]	0x00B3	18	22	△	Yes

List of interrupt information

NOTE: ‘△’: User must clear.



When the chip generates a reset signal, the program starts from the 0x0000 address. When an interrupt signal occurs, the program will jump to the interrupt vector program address to execute the interrupt service routine.

7.2. Interrupt Function

7.2.1. Interrupt Response

When an interrupt request, CPU according to the interrupt vectors determine the type of interrupt service routine (ISR) to run. CPU complete execution ISR, unless a higher priority interrupt source applying for a break. After each ISR has RETI (return from interrupt) instruction. After RETI instruction, CPU continues to execute the program before the interrupt did not happen.

ISR can only be a higher priority interrupt request interrupt. That is, the low-priority ISR can be interrupted by a high-priority interrupt request.

The BF7515CM44-LJTX response interrupt request until the current instruction finished. If the RETI instruction is being executed or read IP, IEN register, after an additional instruction then respond the interrupt request.

7.2.2. Interrupt Priority

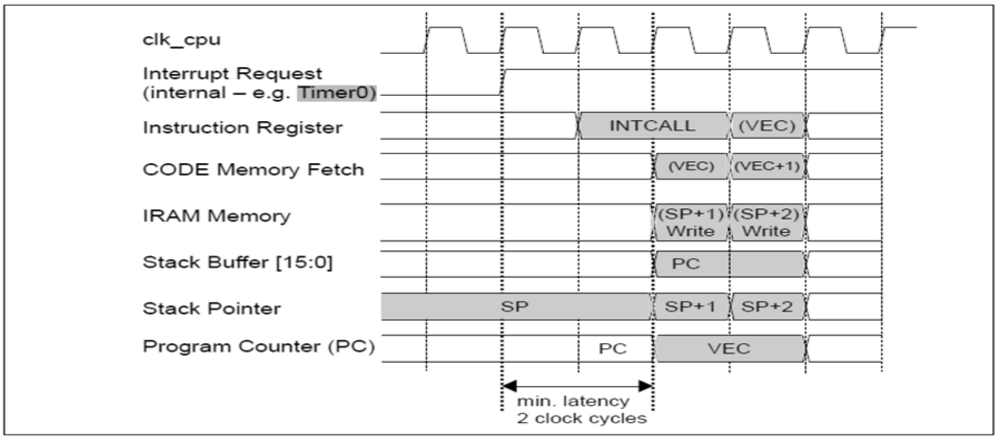
The BF7515CM44-LJTX have two interrupt priority levels: interrupt level and the default priority.Interrupt level (top, high and low) override the default priority. The priority set to high is the first to respond. When the priority is set to the same level, the response will be queued by default. Power-down interrupt is the only high-level interrupt source if allowed. All interrupt sources can be set to high priority or low priority.

Each interrupt source can be assigned a priority level (high or low), and the default priority. The same level of interrupt sources (such as both high priority) the priority is the default priority decision. Interrupt service routine in progress can only be a high-priority interrupt request interrupt.

7.2.3. Interrupt Sampling

Internal modules such as internal timers and serial ports generate interrupt requests through interrupt flag bits in their respective SFR. When the first clock cycle (C1) of each instruction cycle ends, the External Interrupt is sampled on the rising edge of the clock.

In order to ensure that the edge-triggered interrupt is detected, the corresponding port must first maintain the high level of 2 clocks, and then keep the low level of 2 clocks. The following figure shows the timing diagram of interrupt sampling:



7.2.4. Interrupt Wait

Interrupt response time is determined by current state. Fastest response time is five instruction cycles: one cycle to detect the interrupt request, the other 4 used to execute long call (LCALL) to ISR.

When the system is executing a RETI instruction and is followed by a MUL or DIV instruction, the interrupt waits for the longest time (13 instruction cycles). This 13 instruction cycles are as follows: one cycle to detect the interrupt request, three to complete the RETI, five used to execute DIV or MUL instruction, 4 used to execute long call (LCALL) to ISR. In this case, the response time is 13 clock cycles.

7.3. Interrupt Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x88	TCON	RW	0000_0x0xb	Timer control register
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register 0
0xC7	EXINT_STAT	RW	0000_0000b	External interrupt status register
0xD5	INT_POBO_STAT	RW	xxxx_xx00b	LVDT boost/buck interrupt status register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register 2
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register 1
0xFA	PWM_INT_CTRL	RW	xxxx_xx00b	PWM interrupt enable control register

List of interrupt SFR registers

7.3.1. Interrupt enable register

IEN0 (A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit. 0: Mask all interrupts (EA has priority over the respective interrupt enable bits of the interrupt sources); 1: The interrupt is turned on. Whether the interrupt request of each interrupt source is allowed or forbidden is determined by the respective enable bit.
6~4	--	Reserved
3	ET1	Timer 1 overflow interrupt enable bit 0: Disable timer 1 (TF1) to apply for interrupt; 1: Allow TF1 flag bit to request interrupt.

2	EX1	INT_EXT1 enable bit. 0: Disable INT_EXT1 to apply for interrupt; 1: Allow INT_EXT1 to apply for interrupt.
1	ET0	Timer 0 overflow interrupt enable bit 0: Disable timer 0 (TF0) to apply for interrupt; 1: Allow TF0 flag bit to request interrupt.
0	EX0	INT_EXT0 enable bit 0: Disable INT_EXT0 to apply for interrupt; 1: Allow INT_EXT0 to apply for interrupt.

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2/PWM0 interrupt enable 1: WDT/Timer2/PWM0 interrupt enable; 0: WDT/Timer2/PWM0 interrupt disable
6	EX6	LED/LCD interrupt enable 1: LED/LCD enable; 0: LED/LCD disable
4	EX4	ADC interrupt enable 1: ADC interrupt enable; 0: ADC interrupt disable
3	EX3	IIC interrupt enable 1: IIC interrupt enable; 0: IIC interrupt disable
2	EX2	External Interrupt2 interrupt enable 1: External Interrupt2 interrupt enable; 0: External Interrupt2 interrupt disable
5, 1~0	-	Reserved

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	EX15	External Interrupt4 interrupt enable 1: External Interrupt4 interrupt enable;

		0: External Interrupt4 interrupt disable
6	EX14	External Interrupt3 interrupt enable 1: External Interrupt3 enable; 0: External Interrupt3 disable
5	EX13	SPI interrupt enable 1: SPI interrupt enable; 0: SPI interrupt disable
4	EX12	Timer3 interrupt enable 1: Timer3 interrupt enable; 0: Timer3 interrupt disable
3	EX11	UART1 interrupt enable 1: UART1 interrupt enable; 0: UART1 interrupt disable
2	EX10	UART0 interrupt 1: UART0 enable; 0: UART0 disable
1	EX9	LVDT interrupt enable 1: LVDT interrupt enable; 0: LVDT interrupt disable
0	EX8	UART2 interrupt enable 1: UART2 interrupt enable; 0: UART2 interrupt disable

PWM_INT_CTRL (FAH) PWM interrupt enable control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	--	PWM1 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disable
0	--	PWM0 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disabled

7.3.2. Interrupt Priority Register

IPL0 (B8H) Interrupt priority register0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W

Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7~4	–	Reserved
3	PT1	TF1 (Timer1 interrupt) priority selection bit. 0: Timer1 interrupt is low priority; 1: Timer1 interrupt is high priority
2	PX2	INT_EXT1 interrupt priority selection bit. 0: External Interrupt1 is low priority; 1: External Interrupt1 is high priority
1	PT0	TF0 (Timer0 interrupt) priority selection bit. 0: Timer0 interrupt is low priority; 1: Timer0 interrupt is high priority
0	PX0	INT_EXT0 interrupt priority selection bit. 0: External Interrupt0 is low priority; 1: External Interrupt0 is high priority

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	IPL2.7	External Interrupt4 priority selection bit. 1: External Interrupt4 interrupt is high priority; 0: External Interrupt4 interrupt is low priority
6	IPL2.6	External Interrupt3 priority selection bit. 1: External Interrupt3 interrupt is high priority; 0: External Interrupt3 interrupt is low priority
5	IPL2.5	SPI priority selection bit. 1: SPI interrupt is high priority; 0: SPI interrupt is low priority
4	IPL2.4	Timer3 priority selection bit. 1: Timer3 interrupt is high priority; 0: Timer3 interrupt is low priority
3	IPL2.3	UART1 priority selection bit. 1: UART1 interrupt is high priority; 0: UART1 interrupt is low priority
2	IPL2.2	UART0 priority selection bit. 1: UART0 interrupt is high priority;

		0: UART0 interrupt is low priority
1	IPL2.1	LVDT priority selection bit. 1: LVDT interrupt is high priority; 0: LVDT interrupt is low priority
0	IPL2.0	UART2 priority selection bit. 1: UART2 interrupt is high priority; 0: UART2 interrupt is low priority

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit 1: WDT/Timer 2/PWM0 interrupt is high priority; 0: WDT/Timer 2/PWM0 interrupt is low priority
6	IPL1.6	LED/LCD interrupt priority bit 1: LED/LCD interrupt is high priority; 0: LED/LCD interrupt is low priority
4	IPL1.4	ADC interrupt priority bit 1: ADC interrupt is high priority; 0: ADC interrupt is low priority
3	IPL1.3	IIC interrupt priority bit 1: IIC interrupt is high priority; 0: IIC interrupt is low priority
2	IPL1.2	External Interrupt2 interrupt priority bit 1: External Interrupt2 is high priority; 0: External Interrupt2 is low priority
5, 1~0	--	Reserved

7.3.3. Interrupt Flag Register

TCON (88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description

7	TF1	Timer 1 overflow flag The hardware is set to 1 when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable Set to 1, start Timer1 or start Time0 mode, TH0 count at three o'clock
5	TF0	Timer 0 overflow flag Set by hardware when Timer0 overflows
4	TR0	Timer0 start enable Start Timer0 counting when set to 1
3	IE1	External Interrupt1 flag Set by hardware, clear by software
1	IE0	External Interrupt0 flag Set by hardware, clear by software
0, 2	--	Reserved

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	IE15	External Interrupt4 interrupt flag 1: With External Interrupt4 interrupt flag 0: Clear External Interrupt4 interrupt flag
6	IE14	External Interrupt3 interrupt flag 1: With External Interrupt3 interrupt flag 0: Clear External Interrupt3 interrupt flag
5	IE13	SPI interrupt flag 1: With SPI interrupt flag 0: Clear SPI interrupt flag
4	IE12	Timer3/PWM1 interrupt flag 1: With Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag
3	IE11	UART1 interrupt flag 1: UART1 interrupt flag is present 0: Clear UART1 interrupt flag
2	IE10	UART0 interrupt flag 1: There is UART0 interrupt flag 0: Clear UART0 interrupt flag

1	IE9	LVDT interrupt flag 1: With LVDT interrupt flag 0: Clear LVDT interrupt flag
0	IE8	UART2 interrupt flag 1: UART2 interrupt flag 0: Clear LVDT interrupt flag

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag 1: With WDT/Timer2/PWM0 interrupt flag; 0: Clear WDT/Timer2/PWM0 interrupt flag
6	IE6	LED/LCD interrupt flag 1: With LED interrupt flag 0: Clear LED interrupt flag
4	IE4	ADC interrupt flag 1: With ADC interrupt flag; 0: Clear ADC interrupt flag
3	IE3	IIC interrupt flag 1: With IIC interrupt flag; 0: Clear IIC interrupt flag
2	IE2	External Interrupt2 interrupt flag 1: With External Interrupt2 interrupt flag; 0: Clear External Interrupt2 interrupt flag
5, 1~0	–	Reserved

7.3.4. Interrupt Status Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	INT_PWM1_STAT	PWM1 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM1 channel 1: Interrupt is valid; 0: Interrupt is invalid
6	INT_TIMER3_STAT	TIMER3 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER3_CFG, 1: Interrupt is valid; 0: Interrupt is invalid
5	INT08_STAT	INT08 port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT08_IO_SEL=0, 1: Interrupt is valid; 0: Interrupt is invalid
4	INT_WDT_STAT	WDT interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing WDT_CTRL, 1: Interrupt is valid; 0: Interrupt is invalid
3	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is cleared by writing 0, and can also be cleared by writing TIMER2_CFG, 1: Interrupt is valid; 0: Interrupt is invalid
2	INT_PWM0_STAT	PWM0 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM0 channel. 1: Interrupt is valid; 0: Interrupt is invalid
1	INT_LCD_STAT	LCD interrupt status mark, write 0 to clear this bit, write SCAN_START operation can also be cleared, 1: Interrupt is valid; 0: Interrupt is invalid
0	INT_LED_STAT	LED interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START, 1: Interrupt is valid; 0: Interrupt is invalid

EXINT_STAT (C7H) External interrupt status register

Bit number	7	6	5	4
Symbol	INT07_STAT	INT06_STAT	INT05_STAT	INT04_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT03_STAT	INT02_STAT	INT01_STAT	INT00_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT0x_STAT (x=7~0)	INT0x port interrupt status, this bit is cleared by writing 0, and it can also be cleared by writing INT0x_IO_SEL=0 1: interrupt is valid; 0: interrupt is invalid

INT_POBO_STAT(D5H) LVDT boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT boost interrupt status 1: Boost interrupt is valid; 0: Boost interrupt is invalid
0	INT_BO_STAT	LVDT boost interrupt status 1: Boost interrupt is valid; 0: Boost interrupt is invalid

7.4. Secondary Bus Register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register 1
0x35	PERIPH_IO_SEL2	RW	0000_0000b	External port function selection register 2
0x36	PERIPH_IO_SEL3	RW	1xxx_xxxxb	External port function selection register 3
0x37	PERIPH_IO_SEL4	RW	0xxx_x000b	External port function selection register 4
0x38	PERIPH_IO_SEL5	RW	0000_0000b	External port function selection register 5
0x39	EXT_INT_CON1	RW	0101_0101b	External Interrupt configuration register 1
0x3A	EXT_INT_CON2	RW	xxxx_x001b	External Interrupt configuration register 2

List of interrupt secondary bus registers

7.4.1. External Port Function Selection Register

PERIPH_IO_SEL1 (34H) External port function selection register 1

Bit number	7	6	5	4
Symbol	UART1_IO_SEL	UART0_IO_SEL		IIC_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1
Bit number	3	2	1	0
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INT0_8_IO_SEL

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
3	INT3_IO_SEL	INT3 port selection enable 1: INT3 function is selected; 0: INT3 function is not selected
2	INT2_IO_SEL	INT2 port selection enable 1: INT2 function is selected; 0: INT2 function is not selected
1	INT1_IO_SEL	INT1 port selection enable 1: select INT1 function; 0: not select INT1 function
0	INT0_8_IO_SEL	INT0_8 port selection enable 1: INT function is selected; 0: INT function is not selected

PERIPH_IO_SEL2 (35H) External port function selection register 2

Bit number	7	6	5	4
Symbol	INT0_7_IO_SEL	INT0_6_IO_SEL	INT0_5_IO_SEL	INT0_4_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT0_3_IO_SEL	INT0_2_IO_SEL	INT0_1_IO_SEL	INT0_0_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~0	INT0_x_IO_SEL (x=7~0)	INT0_x port selection enable 1: INT function is selected; 0: INT function is not selected

PERIPH_IO_SEL3 (36H) External port function selection register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	INT4_7_IO_SEL	-	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-	-
Reset value	0	-	-	-	-	-	-	-

Bit number	Bit symbol	Description
7	INT4_7_IO_SEL	INT4_7 port selection enable 1: INT function is selected; 0: INT function is not selected
6~0	--	Reserved

PERIPH_IO_SEL4 (37H) External port function selection register 4

Bit number	7	6~3	2	1	0
Symbol	INT4_15_IO_SEL	-	INT4_10_IO_SEL	INT4_9_IO_SEL	INT4_8_IO_SEL
R/W	R/W	-	R/W	R/W	R/W

Reset value	0	-	0	0	0

Bit number	Bit symbol	Description
7, 2~0	INT4_x_IO_SEL (x=15, 10~8)	INT4_x port selection enable 1: INT function is selected; 0: INT function is not selected
6~3	--	Reserved

PERIPH_IO_SEL5 (38H) External port function selection register 5

Bit number	7	6	5	4
Symbol	-	INT4_22_IO_SEL	INT4_21_IO_SEL	INT4_20_IO_SEL
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	INT4_19_IO_SEL	INT4_18_IO_SEL	INT4_17_IO_SEL	INT4_16_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	--	Reserved
6~0	INT4_x_IO_SEL (x=22~16)	INT4_x port selection enable 1: INT function is selected; 0: INT function is not selected

7.4.2. External Interrupt configuration register

EXT_INT_CON1 (39H) External Interrupt configuration register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	INT3_POLARITY		INT2_POLARITY		INT1_POLARITY		INT08_POLARITY	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	1	0	1	0	1

Bit number	Bit symbol	Description
7~6	INT3_POLARITY	External Interrupt3 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
5~4	INT2_POLARITY	External Interrupt2 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
3~2	INT1_POLARITY	External Interrupt1 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode)

		10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)
1~0	INT08_POLARITY	External Interrupt0_8 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)

EXT_INT_CON2 (3AH) External Interrupt configuration register 2

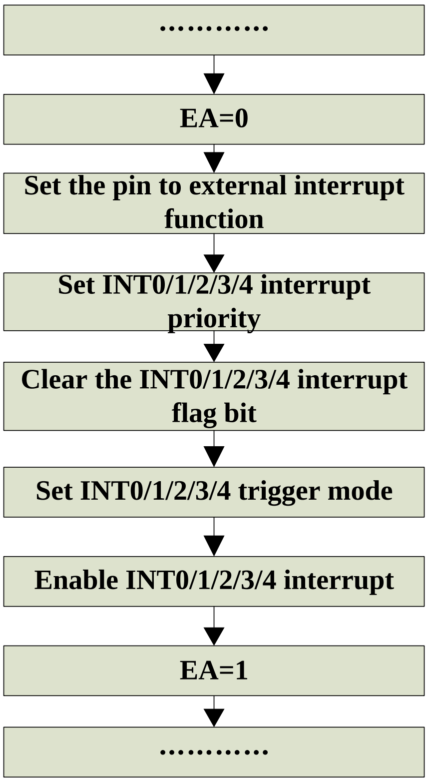
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	INT4_POLARITY	INT0_POLARITY	
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	1

Bit number	Bit symbol	Description
2	INT4_POLARITY	External Interrupt4_x trigger polarity selection: 1: Rising edge (high level wake-up in Sleep mode) 0: Falling edge (low-level wake-up in Sleep mode)
1~0	INT0_POLARITY	External Interrupt0_0~0_7 trigger polarity selection: 01: Falling edge (low-level wake-up in Sleep mode) 10: Rising edge (high level wake-up in Sleep mode) 00/11: Double edge (low-level wake-up in Sleep mode)

Note:

INT4X shares an interrupt vector, and can only respond to one External Interrupt at the same time. When the rising or falling edge of the multi-channel pin External Interrupt is triggered, the external Interrupt pins must be released during the detection process to respond to the current trigger. Signal (when the falling edge is triggered, the release is high, when the rising edge is triggered, the release is low).

7.5. External Interrupt Configuration Process



INT configuration flow chart

8. Timer

The BF7515CM44-LJTX series contains 2 timers (Timer0, Timer1) and 2 external Timers (Timer2, 3) inside the core. Each Timer contains a 16-bit register. When accessed, it appears in the form of two bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The registers of Timer2 are the low byte TIMER2_SET_L and the high byte TIMER2_SET_H. The registers of Timer3 are the low byte TIMER3_SET_L and the high byte TIMER3_SET_H.

The features of Timer are as follows:

- 16-bit Timer0/1/3, 32-bit Timer2;
- Timer0 clock source: f_{SYS}, the internal frequency of the timer clock is f_{SYS} 1/12;
- Timer1 clock source: f_{SYS}, the internal frequency of the timer clock is f_{SYS} 1/12;
- Timer2 clock source: LIRC 32kHz or XTAL 32768Hz/4MHz;
- Timer3 is connected to PLL 24MHz, the internal part of the clock is System clock 1/12 or 1/4;
- Timer0 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer1 supports 8bits automatic reload timing, 16bits manual reload timing function;
- Timer2 supports 32bits automatic reload timing and manual reload timing, and supports interrupt wake-up function;
- Timer3 supports 16bits automatic reload timing, manual reload timing function.

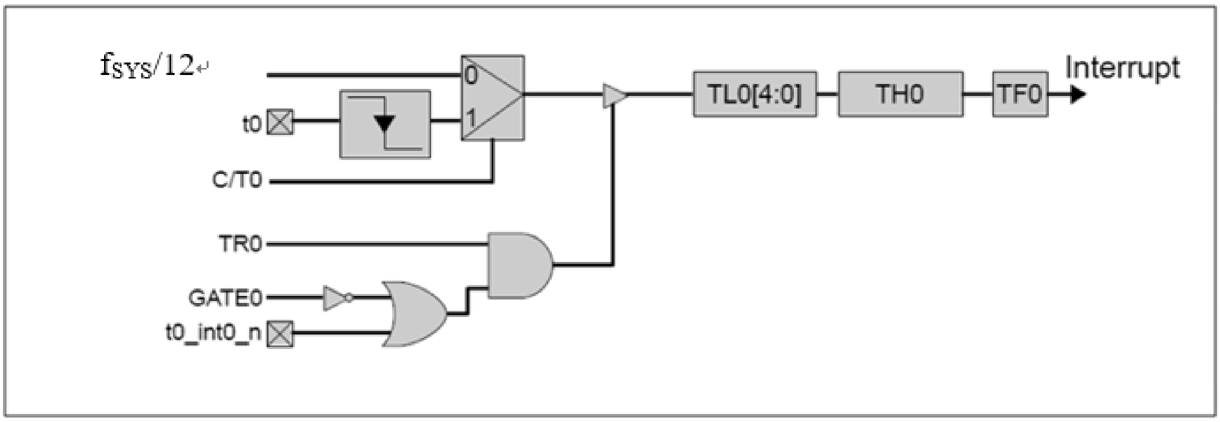
8.1. Timer0 and Timer1

Timer 0/1 has four operating modes, which are controlled by TMOD SFR and TCON SFR.

The four modes of Timer 0/1 are as follows:

- Mode 0: 13-bit timer
- Mode 1: 16-bit timer
- Mode 2: 8-bit timer with automatic reloading of initial value
- Mode 3: Two 8-bit timers

Mode 0: 13-bit timer

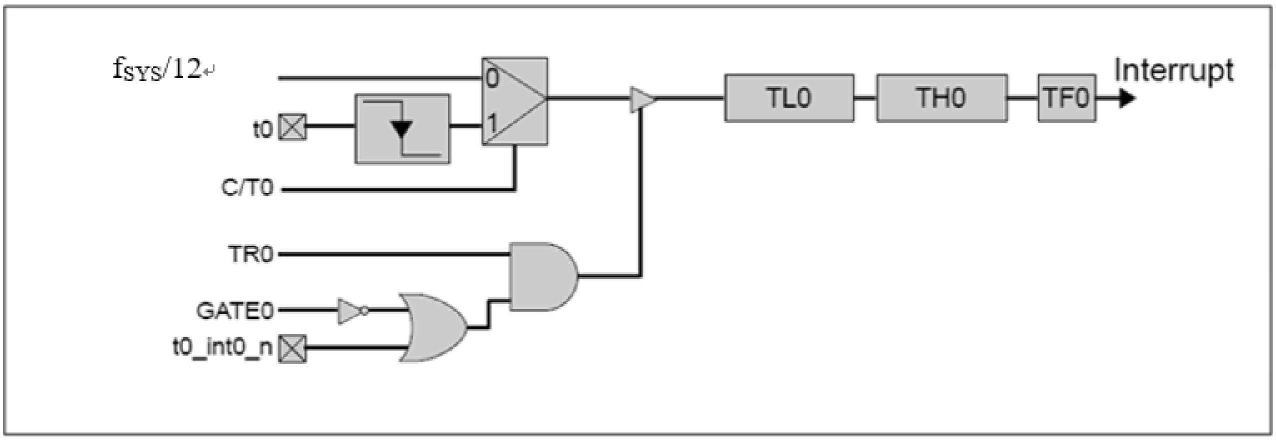


Mode 0 logical structure diagram

As shown in the figure, the working process of timer 0 and timer 1 is the same. In mode 0, Timer 0 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH0 and the lower 5 bits of TL0. Timer 1 is a 13-bit counter, and the 13-bit register consists of 8 bits of TH1 and the lower 5 bits of TL1. The upper three bits of TL0 and TL1 should be ignored. The enable bit (TR0/TR1) in the TCON register controls the on and off of the timer.

The timer counts the selected System clock source ($f_{SYS}/12$). When the 13-bit counter counts up to all 1, the counter is cleared to 0 (all 0), and TF0 (or TF1) is set. t0/t1, C/T0 and C/T1 are all 0, t0_int0_n/t1_int1_n are all 1, and counting enable is only determined by TR0/1.

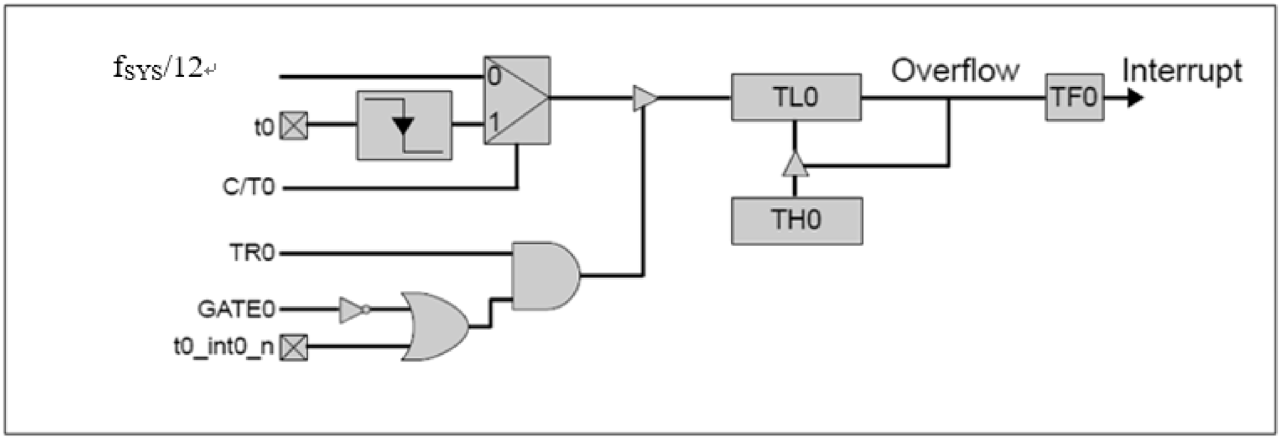
Mode 1: 16-bit timer



Mode 1 logical structure diagram

As shown in the figure, Mode 1 of Timer 0 and Timer 1 are the same. In Mode 1, Timer 0 and Timer 1 are 16-bit counters. The 16-bit register consists of 8 bits TH0 and 8 bits TL0. When the counter counts up to 0xFFFF, the counter is cleared to all 0s. Otherwise, mode 1 and mode 0 are the same. t0/t1, C/T0, C/T1 are all 0, t0_int0_n/t1_int1_n are all 1, and counting enable is only determined by TR0/1.

Mode 2: 8-bit timer with automatic reloading of initial value



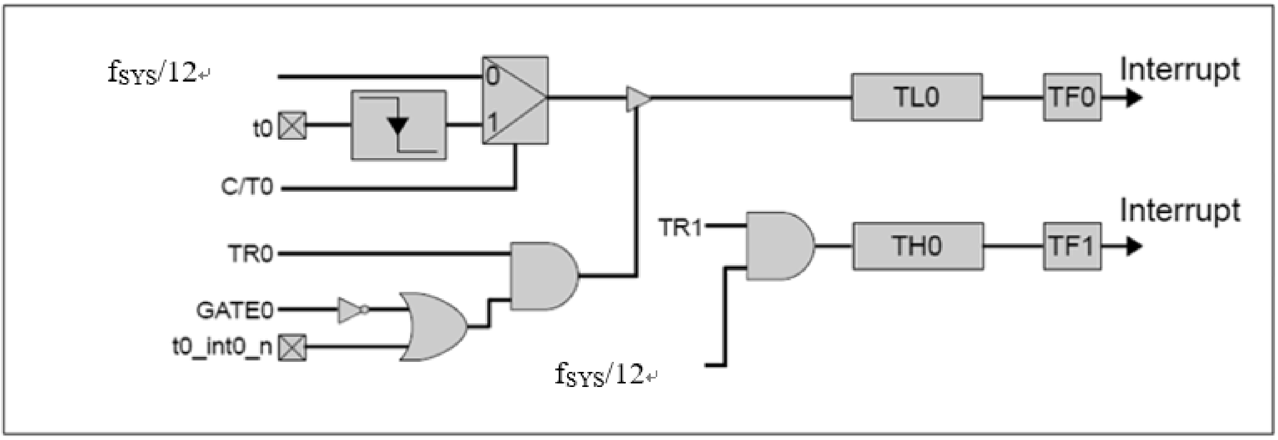
Mode 2 logical structure diagram

Mode 2 of Timer 0 and Timer 1 are the same. In mode 2, the timer is an 8-bit counter with an automatic reload initial value. This counter is the LSB register (TL0 or TL1), and the initial value that needs to be reloaded is stored in the MSB register (TH0 or TH1).

As shown in the figure, the counter control of Mode 2 is the same as Mode 0 and Mode 1.

However, in mode 2, when TLn accumulates to FFh, the value stored in THn is reloaded to TLn. t0/t1, C/T0, C/T1 are all 0, t0_int0_n/t1_int1_n are all 1, and counting enable is only determined by TR0/1.

Mode 3: Two 8-bit timers



Mode 3 logical structure diagram

In mode 3, Timer 0 is two 8-bit timers, at this time Timer 1 stops counting and saves its value. As shown in Figure 5, TL0 is an 8-bit register controlled by the timer 0 control bit. The counter uses GATE as the enable terminal to control the INT_EXT signal reception.

TH0 is a separate 8-bit timer. TH0 can only be used to calculate the clock period (divide by 12). The control bit and flag bit (TR1 and TF1) of Timer 1 are used as the control bit and flag bit of TH0.

When Timer 0 works in Mode 3, the use of Timer 1 is restricted, because Timer 0 uses the control bit (TR1) and interrupt flag (TF1) of Timer 1. Timer 1 can still be used to generate the baud rate, and the value of Timer 1 in the TL1 and TH1 registers is still valid.

When timer 0 works in mode 3, timer 1 is controlled by the mode bit of timer 1. To start timer 1, you need to set timer 1 to mode 0, 1, or 2. To turn off timer 1, set the mode of timer 1 to 3. Timer 1 can be used as a timer (clock is clk/12), but because TR1 and TF1 are borrowed, overflow interrupts cannot be generated. When timer 0 is working in mode 3, the GATE of timer 1 is valid. t0/t1, C/T0, C/T1 are all 0, t0_int0_n/t1_int1_n are all 1, and counting enable is only determined by TR0/1.

8.1.1. Timer0/1 Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x88	TCON	RW	0000_0x0xb	Timer control register
0x89	TMOD	RW	xx00_xx00b	Timer mode register
0x8A	TL0	RW	0000_0000b	Timer 0 counter low 8 bit
0x8B	TL1	RW	0000_0000b	Timer 1 counter low 8 bit
0x8C	TH0	RW	0000_0000b	Timer 0 counter high 8 bit
0x8D	TH1	RW	0000_0000b	Timer 1 counter high 8 bit
0xA8	IEN0	RW	0xxx_0000b	Interrupt enable register
0xB8	IPL0	RW	xxxx_0000b	Interrupt priority register0

Timer0/1 SFR register list

8.1.1.1. Timer Control Register

TCON (88H) Timer control register

Bit number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset value	0	0	0	0	0	-	0	-

Bit number	Bit symbol	Description
7	TF1	Timer 1 overflow flag bit, set by hardware when Timer1 overflows, or TH0 of Timer0 overflows in mode 3.
6	TR1	Timer1 start enable, when set to1, start Timer1, or start Time0 mode three, TH0 count.
5	TF0	Timer 0 overflow flag, set by hardware when Timer0 overflows.
4	TR0	Timer0 start enable, set to 1 to start Timer0 counting.

8.1.1.2. Timer Mode Register

TMOD (89H) Timer mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	M1[1:0]		-	-	M0[1:0]	
R/W	-	-	R/W		-	-	R/W	
Reset value	-	-	0	0	-	-	0	0

Bit number	Bit symbol	Description

7~6, 3~2	--	Reserved
5~4	M1[1:0]	Timer 1 mode selection bit 00: Mode 0–13-bit timer 01: Mode 1–16-bit timer 10: Mode 2–8-bit timer with automatic reloading of initial value 11: Mode 3–two 8-bit timers
1~0	M0[1:0]	Timer 0 mode selection bit 00: Mode 0–13-bit timer 01: Mode 1–16-bit timer 10: Mode 2–8-bit timer with automatic reloading of initial value 11: Mode 3–two 8-bit timers

8.1.1.3. Timer 0 Timer

TL0 (8AH) Timer 0 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL0[7:0]							
R/W	R/W							
Reset value	0							

TH0 (8CH) Timer 0 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH0[7:0]							
R/W	R/W							
Reset value	0							

8.1.1.4. Timer 1 Timer

TL1 (8BH) Timer 1 timer low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TL1[7:0]							
R/W	R/W							
Reset value	0							

TH1 (8DH) Timer 1 timer high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TH1[7:0]							
R/W	R/W							
Reset value	0							

8.1.1.5. Interrupt Enable Register

IEN0 (A8H) Interrupt enable register

Bit number	7	6	5	4	3	2	1	0
Symbol	EA	-	-	-	ET1	EX1	ET0	EX0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value	0	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
7	EA	Interrupt enable bit 0: Mask all interrupts (EA takes precedence over the respective interrupt enable bits of the interrupt sources); 1: Interrupts are enabled. Whether the interrupt request of each interrupt source is allowed or disabled is determined by the respective enable bit.
3	ET1	Timer1 interrupt enable bit 0: Disable Timer 1 to request interrupt; 1: Allow Timer 1 to request interrupt.
1	ET0	Timer 0 interrupt enable bit 0: Disable timer 0 (TF0) from requesting interrupt; 1: Enable TF0 flag bit to request interrupt.

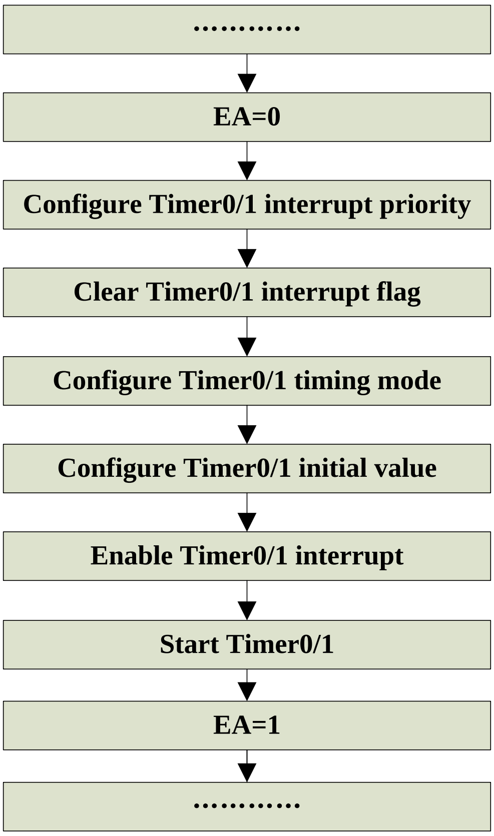
8.1.1.6. Interrupt Priority Register 0

IPL0 (B8H) Interrupt priority register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PT1	PX2	PT0	PX0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PT1	Timer1 interrupt priority selection bit. 0: Timer1 interrupt is low priority; 1: Timer1 interrupt is high priority
1	PT0	Timer0 interrupt priority selection bit. 0: Timer0 interrupt is low priority; 1: Timer0 interrupt is high priority

8.1.2. Timer0/1 Configure Process



Timer0/1 configure process

8.2. Timer2

Timer2 module plays a timing role. The internal main structure of the Timer2 module is a 32-bit counter. The timer function is achieved by counting the input clock.he timer function is achieved by counting the input clock. The counting principle of Timer2 is accumulative counting. An interrupt is generated when the count reaches the set value.

Timer2 count clock can choose external XTAL32768Hz/4MHz and internal low-speed clock LIRC 32kHz, which is determined by clock selection register. Timer2has two working modes: single timer mode and auto-reload mode. In either mode, an interrupt will be generated when the timer is completed.

Configure Timer2 function enable through register TIMER2_EN, TIMER2_RLD configure automatic reload mode or manual reload mode, the timing time is determined by registers TIMER2_SET_L and TIMER2_SET_H. Timer2 supports interrupt wake-up idle mode 1 function. In the interrupt processing function, software is required to clear the interrupt flag.

Timer2 timing duration formula:

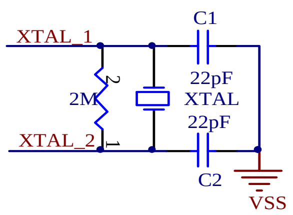
TIMER2_CNT_MOD=0:

$T_{TIMER2}=T_{TIMER2\_CLK}$*({TIMER2_SET_H, TIMER2_SET_L}+1)

TIMER2_CNT_MOD=1:

$T_{TIMER2}=65536*T_{TIMER2\_CLK}$*({TIMER2_SET_H, TIMER2_SET_L}+1)

Note: T_{TIMER2_CLK} = 1/32768 (s) or T_{TIMER2_CLK} = 1/4M(s)



External crystal oscillator circuit reference

Note:

1. Any configuration of TIMER2_SET_H, TIMER2_SET_L, TIMER2_CFG can clear the counter;
2. External crystal oscillator circuit is for reference only, the actual Parameter refers to the crystal oscillator specifications;
3. XTAL 32768Hz excitation power is recommended to be greater than 1μW;
4. XTAL 32768Hz recommends a parallel resistance of 2MΩ;
5. XTAL 4M recommends a parallel resistance of 1MΩ.

8.2.1. Timer2 Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x93	TIMER2_CFG	RW	xxxx_x000b	TIMER2 configuration register
0x94	TIMER2_SET_H	RW	0000_0000b	TIMER2 counter configuration register, high 8 bit.
0x95	TIMER2_SET_L	RW	0000_0000b	TIMER2 counter configuration register, low 8 bit.
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

Timer2 SFR register list

8.2.1.1. TIMER2 Configuration Register

TIMER2_CFG (93H) TIMER2 configuration register

Bit number	7~4	3	2	1	0
Symbol	-	TIMER2_CNT_MOD	TIMER2_CLK_SEL	TIMER2_RLD	TIMER2_EN
R/W	-	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0

Bit number	Bit symbol	Description
3	TIMER2_CNT_MOD	TIMER2 counting step mode selection register 1: The counting step is 65536 clocks 0: The counting step is one clock
2	TIMER2_CLK_SEL	Timer2 clock selection register 1: Select XTAL32768Hz/4MHz 0: Select LIRC
1	TIMER2_RLD	TIMER2 auto reload enable register 1: Auto reload mode 0: Manual reload mode
0	TIMER2_EN	TIMER2 count enable register Configuration 1 start timing, configuration 0 stop timing; In manual reload mode, the hardware will automatically clear this register after the count is completed, stop counting, and in automatic reload mode, the enable register will be maintained after the count is completed, and the count will automatically restart from

		zero. No matter which mode, configuring this register to 1 during the counting process will start counting from zero

8.2.1.2. TIMER2 Count Value Configuration Register

TIMER2_SET_H (94H) TIMER2 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_H[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_H[7:0]	TIMER2 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER2_SET_L (95H) TIMER2 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER2_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER2_SET_L[7:0]	TIMER2 count value configuration register, low 8 bits, the register will re-count when configured during scanning

8.2.1.3. Interrupt Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

3	INT_TIMER2_STAT	TIMER2 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by writing TIMER2_CFG 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2/PWM0 interrupt enable 1: WDT/Timer2/PWM0 interrupt enable; 0: WDT/Timer2/PWM0 interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag 1: WDT/Timer2/PWM0 interrupt flag; 0: Clear WDT/Timer2/PWM0 interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit 1: WDT/Timer 2/PWM0 interrupt is high priority; 0: WDT/Timer 2/PWM0 interrupt is low priority

8.2.2. Timer2 Secondary Bus Register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register

Timer2 List of secondary bus registers

8.2.2.1. Analog Module Switch Register

PD_ANA (2DH) Analog module switch register

Bit number	7	6	5	4	3~1	0
Symbol	-	PD_LVDT	-	PD_XTAL_32K	-	PD_ADC
R/W	-	R/W	-	R/W	-	R/W
Reset value	-	1	-	1	-	1

Bit number	Bit symbol	Description
4	PD_XTAL_32K	PA port crystal oscillator circuit (32768Hz/4MHz) control register 1: Off; 0: On, default off

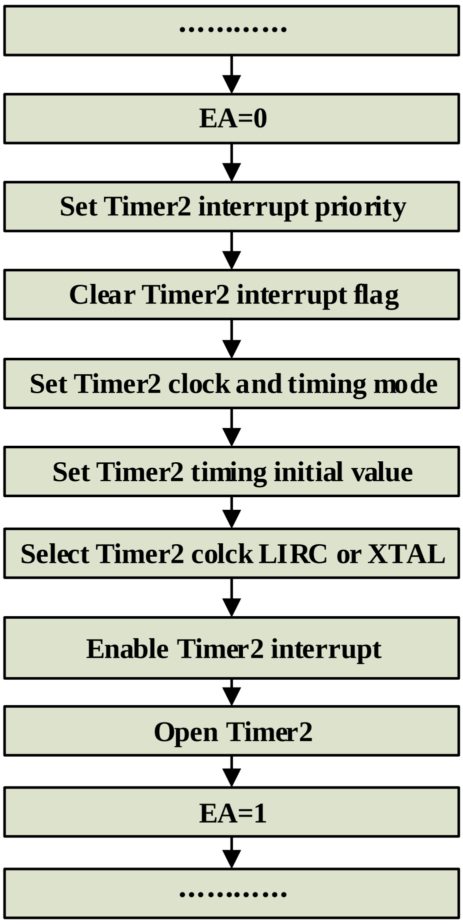
8.2.2.2. Crystal Frequency Selection Register

XTAL_CLK_SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	Crystal frequency selection register 1: Select 4MHz; 0: Select 32768Hz

8.2.3. Timer2 Configure Process



Timer2 configure process table

Timer2 configure process:

1. Configure the timer setting register TIMER2_SET_H/TIMER2_SET_L and step configuration TIMER2_CNT_MOD;
2. Then configure the auto-reload enable register TIMER2_RLD as needed, and set it to 1 if automatic cycle counting is needed, otherwise it is set to 0;
3. Finally, in the configuration timing enable register TIMER2_EN, turn on the timing configuration TIMER2_EN=1;
4. Stop timing: TIMER2_EN=0.

Note:

1. TIMER2_EN=0x01 operation should be placed at the end of all configurations;
2. During the timing of TIMER2, it is forbidden to change the related configuration of Timer2. If you want to modify it, you need to stop the timing first.
3. For precise timing, in the automatic reload mode, the three registers of TIMER2 are not allowed to be configured during interrupt processing.

8.3. Timer3

Timer3 is a 16-bit timer. Configure Timer3 function enable through register TIMER3_EN. TIMER3_RLD configures automatic reload mode or manual reload mode. The timing time is determined by registers TIMER3_SET_L and TIMER3_SET_H.

The timer clock can be divided by 12 or 4 of the 24MHz clock, which is determined by the clock selection register. Timer3 supports the interrupt wake-up idle mode 0 function.

Single timing mode: After a timing is completed, the hardware will automatically pull down TIMER3_EN to stop timing.

Automatic reset mode: The hardware will automatically reload the setting value, and TIMER3_EN will continue to be maintained at 1 to restart the next timing; the software will stop TIMER3 counting by writing 0 to the register TIMER3_EN, or modify the timing mode midway.

The TIMER3 timing duration formula is:

At 12 frequency, $T_{\_TIMER3} = T_{CLK\_24M}$*({TIEMR3_SET_H, TIMER3_SETL} + 1)*12

At 4 frequency, $T_{\_TIMER3} = T_{CLK\_24M}$*({TIEMR3_SET_H, TIMER3_SETL} + 1)*4

Note:

Configure any TIMER3_SET_H, TIMER3_SET_L, TIMER3 _CFG to clear the counter.

8.3.1. Timer3 Related Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x84	TIMER3_CFG	RW	xxxx_x000b	TIMER3 configuration register
0x85	TIMER3_SET_H	RW	0000_0000b	TIMER3 count value configuration register, high 8 bits
0x86	TIMER3_SET_L	RW	0000_0000b	TIMER3 count value configuration register, low 8 bits
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

Timer3 SFR register list

8.3.1.1. TIMER3 Configuration Register

TIMER3_CFG (84H) TIMER3 configuration register

Bit number	7~3	2	1	0
Symbol	-	TIMER3_CLK_SEL	TIMER3_RLD	TIMER3_EN
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
2	TIMER3_CLK_SEL	TIMER3 timing clock selection register. 1: Select clk_24M/4; 0: Select clk_24M/12
1	TIMER3_RLD	TIMER3 auto reload enable register 1: Auto reload mode; 0: Manual reload mode.
0	TIMER3_EN	TIMER3 count enable register Configure 1 to start timing, configure 0 to stop timing In manual reload mode, the hardware will automatically clear this register after the timing is completed. Configure the register during the scan process to re-count.

8.3.1.2. TIMER3 Count Value Configuration Register

TIMER3_SET_H (85H) TIMER3 count value configuration register, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER3_SET_H[7:0]							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	TIMER3_SET_H[7:0]	TIMER3 count value configuration register, high 8 bits, the register will count again when configured during scanning.

TIMER3_SET_L (86H) TIMER3 count value configuration register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	TIMER3_SET_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	TIMER3_SET_L[7:0]	TIMER3 count value configuration register, low 8 bits, the register will re-count when configured during scanning.

8.3.1.3. Interrupt Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	INT_TIMER3_STAT	TIMER3 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by writing TIMER3_CFG 1: Interrupt is valid; 0: Interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
4	IE12	Timer3/PWM1 interrupt enable 1: Timer3/PWM1 interrupt enable; 0: Timer3/PWM1 interrupt disable

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

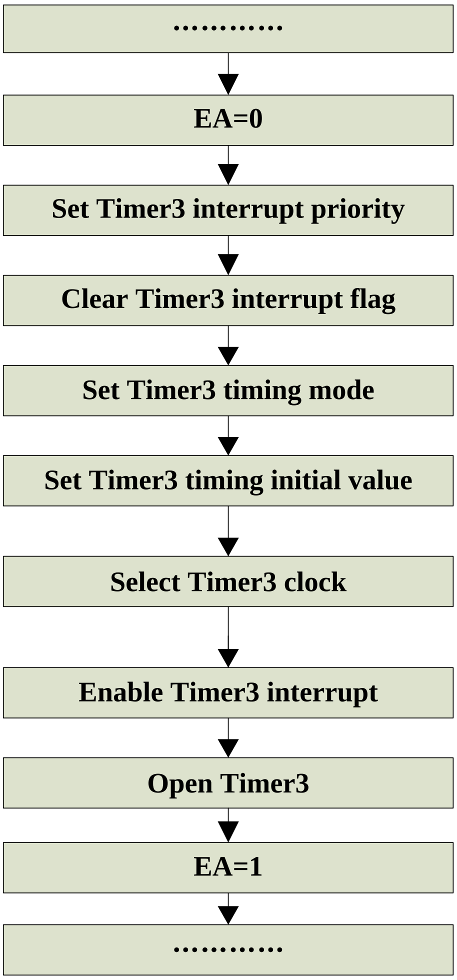
Bit number	Bit symbol	Description
4	EX12	Timer3/PWM1 interrupt enable 1: Timer3/PWM1 interrupt enable; 0: Timer3/PWM1 interrupt disable

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
4	IPL2.4	Timer3/PWM1 priority selection bit. 1: Timer3/PWM1 interrupt is high priority; 0: Timer3/PWM1 interrupt is low priority

8.3.2. Timer3 Configure Process



Timer3 Configuration flow chart

Timer3 Configuration process:

1. Configure the timer setting register TIMER3_SET_H/TIMER3_SET_L and step configuration TIMER3_CNT_MOD;
2. Then configure the auto-reload enable register TIMER3_RLD as needed, and set it to 1 if automatic cycle counting is needed, otherwise it is set to 0;
3. Finally, in the configuration timing enable register TIMER3_EN, turn on the timing configuration TIMER3_EN=1;
4. Stop timing: TIMER3_EN=0.

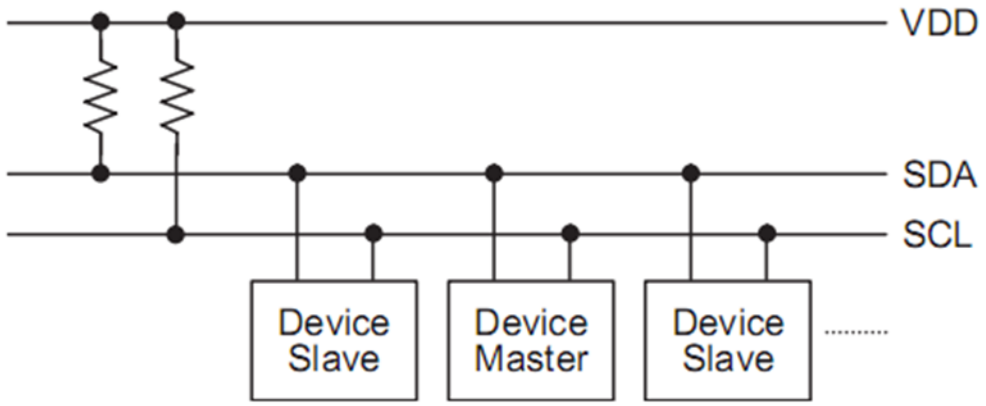
Note:

1. TIMER3_EN=0x01 operation should be placed at the end of all configurations;
2. During the timing of TIMER3, it is forbidden to change the related configuration of Timer.If you want to modify it, you need to stop the timing first;
3. If accurate timing is required, in the automatic reload mode, it is not allowed to configure TIMER3_EN=0x01 during interrupt processing.

9. IIC

The BF7515CM44-LJTX supports standard and fast IIC communication, and has the following characteristics:

- Two serial interfaces: serial data line SDA and serial clock line SCL
- Comply with philips standard communication protocol
- Transmission rate: 100 kHz, 400 kHz
- Support 7-bit address addrring
- With the function of extending the low level of the clock
- The core can be awakened by IIC interrupt in low power mode
- Detect write conflicts and abnormal buffer BUF overflow



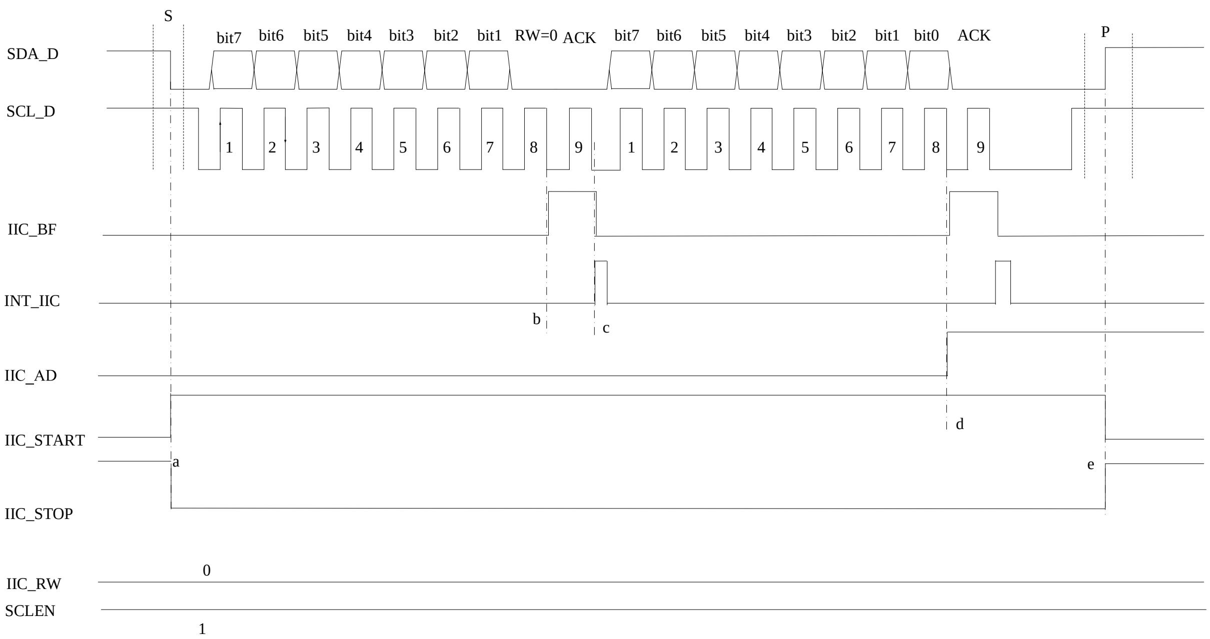
IIC master-slave connection diagram

The master and slave are connected by SCL (serial clock) line and SDA (serial data) line. SCL and SDA must be connected with pull-up resistors (4.7k~10k recommended).

9.1. Communication Timing

The BF7515CM44-LJTX uses hardware slave. When host read /write data, after the slave receives the address, if the address matches, an interrupt is generated and a valid response signal is sent. And an interrupt is generated after the host computer writes the eighth clock of the data, and the host will not generate an interrupt signal when sending the stop signal. IIC timing diagram as follows:

IIC host write timing diagram



IIC write not pull down clock line diagram

As shown in the above figure, the schematic diagram of the clock line is not pulled down during the host write operation. From this, you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a in the figure.

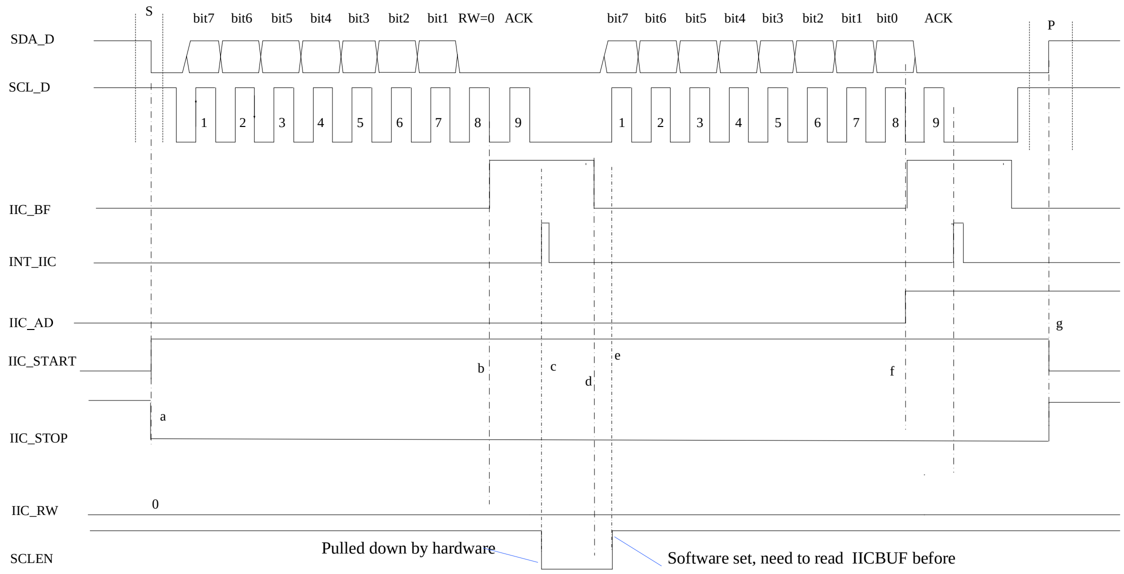
Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b in the figure.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c.The MCU executes interrupt subroutine device needs to read IICBUF. Even if this data is not useful, it needs to be operated.Reading the IICBUF operation will indirectly clear the START_BF.

The host continues to send messages. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set. The currently received byte of the flag is data, and the stop signal has no effect on the IIC_STOP flag. That is, the stop signal IIC_STOP is detected, as shown by the dotted line d. And the IIC_AD flag will not be cleared; The interrupt is generated after the falling edge of the ninth clock, and the interrupt subroutine requires the same operation.

If the host wants to send multiple bytes, it can continue to send. The figure above only shows the case where the host sends a data. Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host write pull low timing diagram



IIC write low clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, and the slave sets the IIC_START status bit after detecting the IIC_START signal, as shown by the dotted line a.

Then the host sends the address bytes and write flag bit, and the slave automatically compares with its own address after receiving the address byte. Set IIC_BF after the falling edge of the eighth clock if the address matches, as shown by the dotted line b. An interrupt signal INT_IIC is generated after the falling edge of the ninth clock, as shown by the dotted line c.

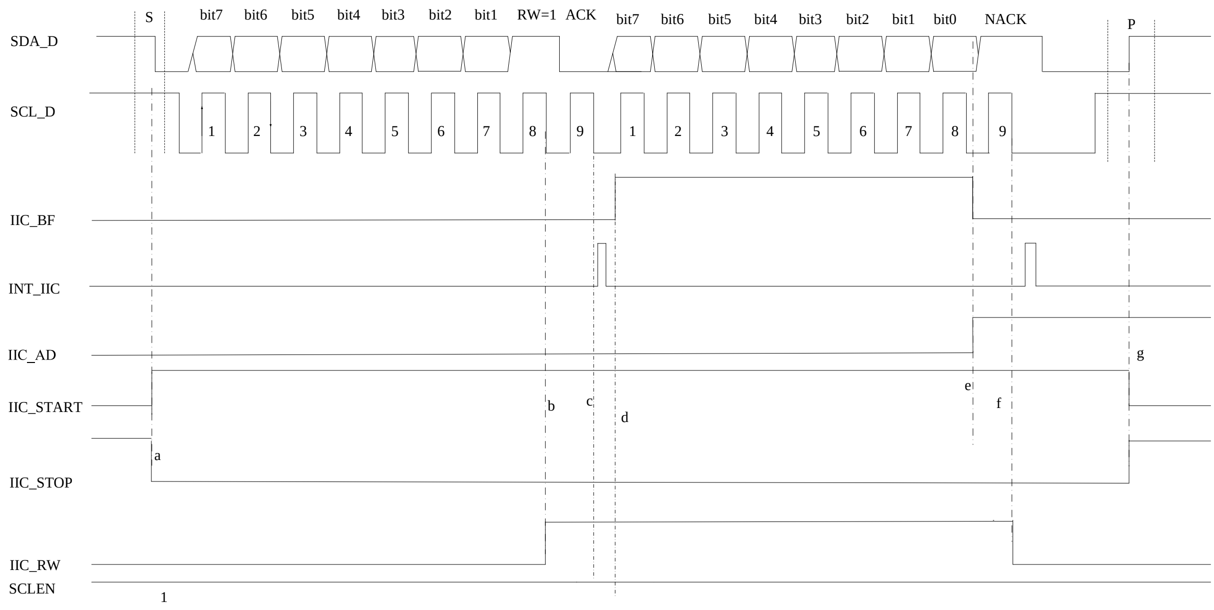
SCLEN will be automatically cleared by hardware after the falling edge of the 9th clock. This process is used to process or read data from the slave. Even if this data is not useful, reading IICBUF will cause IIC_BUF to be cleared indirectly, as shown by the dotted line d. Software sets SCLEN to release the clock line.As shown by the dotted line e.

After the master detects that the slave releases the SCL, it continues to send the synchronous clock. The IIC_BF is also set after the falling edge of the 8th clock of the 2nd byte, and the IIC_AD flag is also set, he currently received byte of the flag is data, as shown by the dotted line f, and the stop signal has no effect on the IIC_STOP flag. Hat is, the stop signal IIC_STOP is detected, and the IIC_AD flag will not be cleared; The interrupt is generated after the falling edge of the ninth clock

If the host wants to send multiple bytes, it can continue to send, as shown in the figure above, it only indicates that the host sends one piece of data. The situation that needs to be noted is that when the host sends the last data, the function of pulling down the clock line is not enabled.

Finally, the host sends a stop signal IIC_STOP after sending all the data, indicating the end of the communication, releasing the IIC bus, and the bus enters the idle state.

IIC host read timing diagram



IIC master reading does not pull down the clock line diagram

As shown in the above figure, it is a schematic diagram of pulling down the clock line during the host write operation, from which you can see the changes of the IIC bus and some internal signal changes.

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address bytes and write flag bit, IIC_RW = 1, indicates that the host reads the slave. In the case of address match, after the falling edge of the eighth clock, the status bit IIC_RW is set. As shown by the dotted line b; If Address does not match, IIC_RW will not be set.

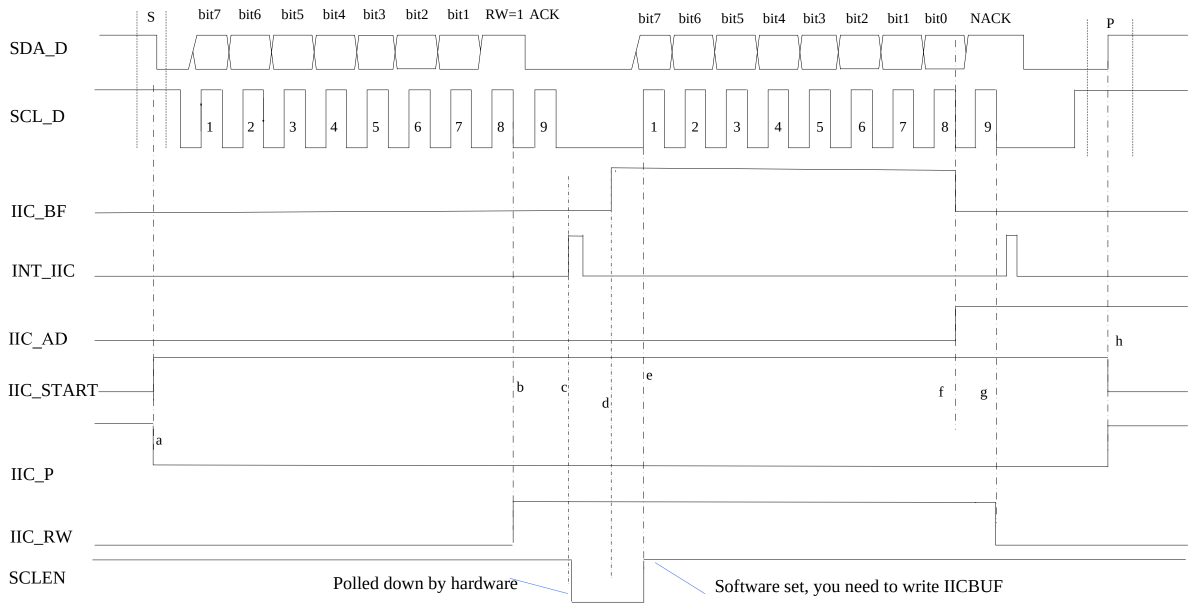
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. Ballast the data in IICBUFFER to IICBUF, IIC is set, as shown by the dotted line d, and the highest bit is sent to the bus. After the eighth clock, one byte of data is sent, IIC_BF is set to clear. At the same time, the address data flag will also be set. As shown by the dotted line e.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate. If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. In the diagram, the host only reads one piece of data, and then responds with NACK, and then sends the IIC_STOP signal to terminate the communication.When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line f.

If the host sends a NACK, the slave SCLEN will not be automatically pulled low.

Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line g. The bus enters the idle state.

IIC host read pull low timing diagram



IIC host read pull low clock line diagram

As shown in the figure above, it is the timing diagram of the master reading the slave clock line low. From the figure, we can know the changes of the bus and the changes of the internal signals of some circuits

First the host sends a start signal IIC_START, marking the beginning of communication. As shown by the dotted line a. The internal circuit detects the IIC_START signal timing and sets the status flag IIC_START.

Then the host sends the address byte after the IIC_START signal. IIC_RW = 1, indicates that the host reads the slave. In the case of Address matching, after the falling edge of the eighth clock, status bit IIC_RW set. As shown by the dotted line b. Will not be set if the addresses do not match

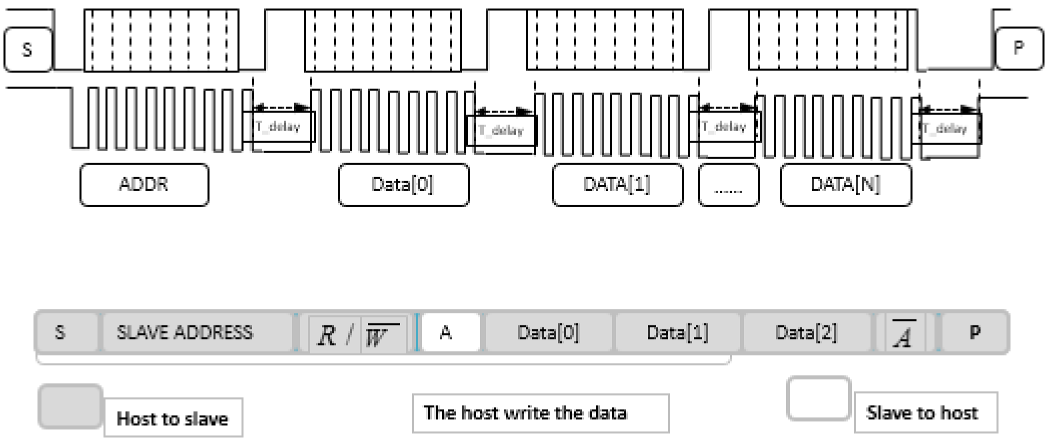
An interrupt signal INT_IIC is generated after the falling edge of the ninth clock. As shown by the dotted line c. SCLEN will also be automatically pulled low by the hardware after the falling edge of the ninth clock. This period is used to process or prepare data from the slave, then write the prepared data to IICBUF, set SCLEN in software, and release the clock line. As shown by the dotted line d. In writing the data to the IICBUF, the IICBUF will be set, indicating that the IIC is full at this time. As shown by the dotted line e. Software sets SCLEN, releases the clock line

After the master detects that the slave releases the SCL, it continues to send the synchronous clock and read the slave data. After the falling edge of the 8th clock, one byte of data has been sent and IIC_BF cleared. At the same time, the address data flag will also be set, indicating the currently transmitted byte data. As shown by the dotted line f.

An interrupt signal INT_IIC is generated after the falling edge of the ninth clock.If the host needs to continue to read the slave, the host replies with a valid acknowledge bit ACK and continues to communicate; If the data require by the host has been read, the host replies with an invalid response NACK, and then sends a stop signal IIC_STOP to stop the communication. When the NACK is detected, the read/write flag IIC_RW is cleared by hardware. As shown by the dotted line g.

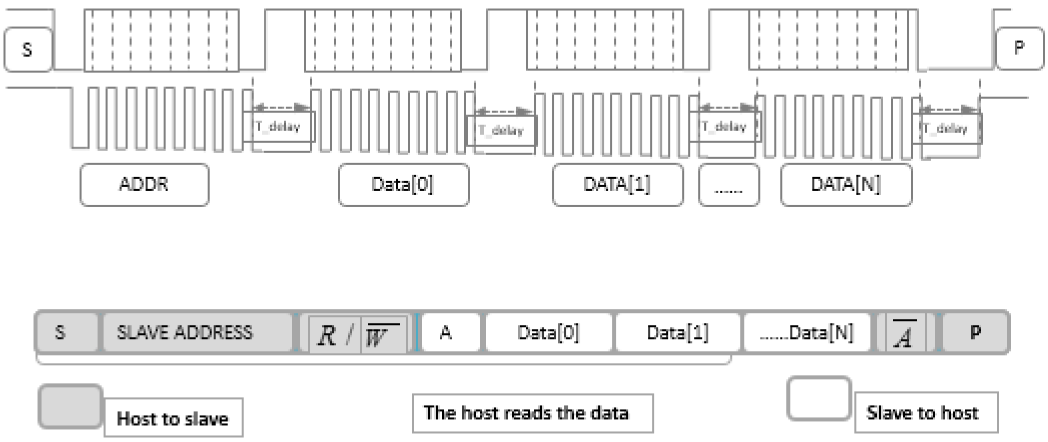
Finally, the host sends a stop signal IIC_STOP after reading all the data, indicating the end of the communication. When the IIC_STOP signal is detected the status bit IIC_STOP is set and IIC_START is cleared. Release IIC bus. As shown by the dotted line h. The bus enters the idle state.

IIC host write data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us .

IIC host read data diagram



PS: T_delay: Reserve slave interrupt time, generally 60us~300us, if the slave IIC interrupts the service processing time at100us, suggest T_delay>200us.

At the eighth clock slave send ack, IIC interrupt occurs at the ninth clock fulling edge. It is recommended that the host delay 60us~300us when the ninth clock fulling edge is sent. Reserve the slave IIC interrupt service data preparation time, and then send the clock signal.

9.2. IIC Port Configuration

The BF7515CM44-LJTX provides secondary bus register PERIPH_IO_SEL1, configure Bit4 of this register to select IIC port.

Write 1 in register PERIPH_IO_SEL1.4, then PE4, PE5 will be configured as IIC function:

SCL0A, PE4 is IIC serial clock line;

SDA0A, PE5 is IIC serial data line.

Write 0 in register PERIPH_IO_SEL1.4, then PC4, PC5 will be configured as IIC function:

SCL0B, PC4 is IIC serial clock line;

SDA0B, PC5 is IIC serial data line.

9.3. IIC Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xE3	IICADD	RW	0000_000xb	IIC address register
0xE4	IICBUF	RW	0000_0000b	IIC transmit receive data register
0xE5	IICCON	RW	xx01_0000b	IIC configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE8	IICSTAT	R/RW	0100_0100b	IIC status register
0xE9	IICBUFFER	RW	0000_0000b	IIC transmit receive data buffer register
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

IIC SFR register list

9.3.1. IIC Address Register

IICADD (E3H) IIC address register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICADD[7:1]							-
R/W	R/W							-
Reset value	0							-

Bit number	Bit symbol	Description
7~1	IICADD[7:1]	IIC address register

9.3.2. IIC Transmit Receive Data Register

IICBUF (E4H) IIC transmit receive data register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUF							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUF	IIC transmit and receive data buffer

The specific application process is as follows:

In the send state, after the data is ballasted into the IICBUF, under the synchronous clock of the host. The data is sequentially shifted and sent out, the high position is in front. After 8 clocks, one byte is sent.

In the receive state, after the host's 8 clocks have passed, the data is written to the BUF. After the 9th clock, an interrupt is generated, telling the CPU to read the data in the IICBUF.

Writing data to IICBUF is conditional, when RD_SCL_EN=1, only IIC_RW=1, and SCLEN=0 can write data into IICBUF; Otherwise, the operation of writing IICBUF is prohibited. That is to say, if the condition is not satisfied, the operation of writing IICBUF cannot be successful, and the data cannot be written. IICBUF data will not change, but will also cause write confilicts.

For example: IICBUF already has been 55h. In case the condition of writing IICBUF is not satisfied, we want to write data 00h into IICBUF. The result is that the data in IICBUF is still 55h, and the write conflict flag IIC_WCOL is set to tell the user that the operation is abnormal.

When RD_SCL_EN=0, the data to be the slave is the value of the ballast IICBUFFER register when the interrupt signal is generated.

9.3.3. IIC Configuration Register

IICCON (E5H) IIC configuration register

Bit number	7	6	5	4
Symbol	-	-	IIC_RST	RD_SCL_EN
R/W	-	-	R/W	R/W
Reset value	-	-	0	1
Bit number	3	2	1	0
Symbol	WR_SCL_EN	SCLEN	SR	IIC_EN
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7~6	--	Reserved
5	IIC_RST	IIC module reset signal 1: IIC module reset operation, 0: IIC module works normally
4	RD_SCL_EN	The host reads the low clock line control bit 1: Enable the host to read and pull down the clock line function, 0: Disable the host read and pull down clock line function
3	WR_SCL_EN	The host writes the low clock line control bit, 1: Enable the function of writing and pulling down the clock line, 0: Disable the function of writing and pulling down the clock line
2	SCLEN	IIC clock enable bit: 1: clock works normally, 0: lows the clock line
1	SR	IIC conversion rate control bit 1: The conversion rate control is turned off to adapt to the standard speed mode (100K); 0: Conversion rate control is enabled to adapt to fast speed mode (400K)
0	IIC_EN	IIC work enable bit 1: IIC works normally 0: IIC does not work

The IICCON register is used to control the communication operation.

IICEN is module enable signal, when IICEN=1, the circuit works.

SR is the conversion rate control bit, SR=1 conversion ratecontrol off, port adapted to 100Kbps communication.

SCLEN is clock enable control bit, although the slave cannot generate the communication clock, the slave can extend the low time of the clock according to the protocol. SCLEN=0, clock line is locked at low level; SCLEN=1, release clock line. The premise of extending the low level of the clock is IICEN=1, otherwise the internal circuit will not have any effect on the IIC bus. SCLEN is often used to extend low time and make the host enter the wait state, so that the slave has enough time to process the data.

WR_SCL_EN is write low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

IIC_RW=0, according to the communication rate of the host and the time of processing the interrupt, it is determinded whether to lower the clock line, that is, configure the WR_SCL_EN bit.

When the CPU can process the interrupt and exit the interrupt within 8 IIC clocks. WR_SCL_EN=0 disable pull down the clock clock line function. At this time, the hardware will not automatically pull down the clock line when the interrupt arrives. When the CPU cannot process the interrupt and exit in the 8 IIC clocks, WR_SCL_EN=1 enables the clock line to be pulled down. At this point, the hardware automatically pulls down the clock line when the interrupt arrives, forcing the host to enter the wait state. When the data written to the IIC is read by the CPU, the software sets SCLEN.

RD_SCL_EN is read low line control bit. When it is 1 to enable the interrupt to pull down the clock line, when it is 0, it does not enable the interrupt to pull down the clock line.

RD_SCL_EN=1, when the slave receives the address byte or sends one byte and the host sends, SCLEN will be automatically pulled low by hardware, forcing the host to the enter the wait state. The release the IIC clock from the slave, the following two operations arerequired: first write the data to be sent to the IIC, set the software in IICBUF in SCLEN. The purpose of this design is to ensure that the data to be sent has been written in the IICBUF before the SCL is pulled high.

RD_SCL_EN=0, when the slave receives the address byte or sends one byte and the host sends an ACK, the slave immediately polls the data prepared in the IICBUFFER register to the transmit buffer register and then to the data line. Therefore, in order to ensure that data transmitted each time is correct, IICBUFFER prepares the next data to be sent in the interrupt service routine. The data received by the host is the last interrupted data, and the first time the data is received is ready for initialization.

Note: When you need to pull down the clock line, that is, WR_SCL_EN/RD_SCL_EN=1. Software should turn off the clock line until the last Byte data is sent and received. That is, WR_SCL_EN/RD_SCL_EN=0, the software should turn on the write low pull clock line before sending and receiving the last Byte data. This kind of operation can be self-regulated according to whether the host is software or hardware.

IIC_RST is IIC module control enable bit, enable the IIC module reset function for 1 and disable the IIC module reset function when 0. Pay attention to configuration 1 reset IIC module all DFF triggers. The reset terminal of IIC_RST is global reset, and the other reset terminal are iic_rst_n. All iic_rst writes 0 first, then operate other register configurations.

9.3.4. IIC Status Register

IICSTAT (E8H) IIC status register

Bit number	7	6	5	4
Symbol	IIC_START	IIC_STOP	IIC_RW	IIC_AD
R/W	R	R	R	R
Reset value	0	1	0	0
Bit number	3	2	1	0
Symbol	IIC_BF	IIC_ACK	IIC_WCOL	IIC_RECOV
R/W	R	R	R/W	R/W
Reset value	0	1	0	0

Bit number	Bit symbol	Description
7	IIC_START	Start signal flag 1: Indicates that the start bit is detected; 0: Indicates that the start bit is not detected.
6	IIC_STOP	Stop signal flag 1: Means in the stop state; 0: Means that the stop bit is not detected.
5	IIC_RW	Read and write flag Record the read/write information obtained from the address byte after the last address match, 1: Indicates read operation; 0: Means write operation.
4	IIC_AD	Address data flag 1: Indicates that the most recently received or sent byte is data; 0: Indicates that the most recently received or sent byte is an address.
3	IIC_BF	IICBUF full flag bit: when receiving in IIC bus mode 1: Indicates that the reception is successful and the buffer is full; 0: Indicates that the reception is not completed and the buffer is still empty When sending in IIC bus mode: 1: Indicates that data transmission is in progress (not including the response bit and stop bit), and the buffer is still full; 0: Indicates that the data transmission has been completed (not including the response bit and stop bit), and the buffer is

		empty.
2	IIC_ACK	Reply flag 1: Indicates an invalid response signal; 0: indicates an effective response signal.
1	IIC_WCOL	Write conflict flag 1: Indicates that when the IIC is sending the current data, new data is trying to be written into the sending buffer; the new data cannot be written into the buffer; 0: No write conflict occurred.
0	IIC_RECOV	Receive overflow flag 1: Indicates that new data is received when the previous data received by IIC has not been taken away, and the new data cannot be received by the buffer; 0: Indicates that no receive overflow has occurred.

IIC status register, used to reflect the status in the communication process, for users to query.

IIC_START: Start signal status bit, IIC_START is set when the start signal is detected, Indicating that the bus is busy.

IIC_STOP: Stop signal status bit, IIC_START is set when the start signal is detected, indicating that the bus is idle. When the start signal is detected, the hardware is cleared, indicating that communication begins.

IIC_AD: Address data flag. It indicates whether the byte currently received or sent is an address or data. IIC_AD =0, flag is currently received or sent byte is the address; IIC_AD = 1 flag is currently received or sent byte is the data; Start signal, stop signal, non-response signal have no effect on this status bit. This status bit change occurs on the falling edge of the eighth clock.

IIC_RW: Read and write flag. The flag bit is recorded the read and write information bits obtained from the address is matched. IIC_RW = 1 means the host reads the slave. RW = 0 means the host writes the slave. Start signal, stop signal, non-answer signal (NACK) is cleared IIC_RW. This status bit change occurs on the falling edge of the eighth clock.

IIC_BF: BUFFER full flag. It indicates that the transceiver buffer is currently full or empty. IIC_BF=0 indicates that the buffer does not receive data and the buffer is empty; IIC_BF=1 indicates that the buffer receive data and the buffer is full. This status bit can only be set and cleared indirectly, not directly.

Address matching and IIC_RW=0, IIC_BF will be set after the falling edge of the eighth clock, indicating that the IICBUF has received the data. The IICBUF should be read during the execution of the interrupt routine, and the read IICBUF will indirectly clear the BF flag. If the host does not read IICBUF and the host continues to send data, a receive overflow will occur. Although the slave still receives the host to send data and is ballasted to the IICBUF.

IIC_RW=1 indicates the operation of the master to read the slave, the slave operation needs to write data to the IICBUF, and the slave writes IICBUF operation to set the IICBUF. The software then sets SCLEN to release the clock line; The host The host sends the synchronous clock. After the

8th clock is passed, the IICBUF is cleared by hardware after the data in the IICBUF is sent out.

IIC_ACK: Answer flag. Regardless of whether the host is a read or write operation, the slave samples the data line from the rising edge of the ninth clock and records the response information. The acknowledge bits are divided into a valid acknowledgment ACK and a non-valid acknowledgement bit NACK. That is to say, the rising edge of the ninth clock samples the data to 0, indicating that the ACK is valid, and the IIC_ACK is cleared. If data 1 is sampled, NACK is set, indicating non-response. After the non-acknowledgment signal, the host will send a stop signal to announce the end of the communication. The start signal will clear this status bit.

IIC_WCOL: Write conflict flag. IICBUF only when IIC_RW=1, RD_SCL_EN=1 and SCLEN=0 can be written by the CPU. Any other attempt to write to IICBUF is forbidden. If the above conditions are not met, the write IICBUF operation occurs. Then the data will not be written to IICBUF, and the conflict flag IIC_WCOL will be set. This flag needs to be cleared by software.

IIC_RECOV: Receive overflow flag.In the case of IICBUF full, that is, in the case of data in the IICBUF. If IIC received new data, it will receive overflow and IIC RECOV will set.At the same time, the data in the IICBUF will not be updated, and the newly received data will be lost. This status bit also requires software to clear, otherwise it will affect the subsequent communication. This kind of situation will only appear in IICRW=0. BF=1, and the CPU will appear when it does not read IICBUF.

9.3.5. IIC Send and Receive Data Buffer Register

IICBUFFER (E9H) IIC send and receive data buffer register

Bit number	7	6	5	4	3	2	1	0
Symbol	IICBUFFER							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	IICBUFFER	IIC transmit and receive data buffer register; when RD_SCL_EN is 0, when the master reads data, the data in IICBUFFER will be sent to the slave send buffer register 2 clocks after the interrupt, as the data sent by the slave. So prepare IICBUFFER interrupt data before interrupt generation.

9.3.6. Interrupt Register

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-

Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
3	EX3	IIC interrupt enable 1: IIC interrupt enable; 0: IIC interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
3	IE3	IIC interrupt flag 1: IIC interrupt flag is present; 0: IIC interrupt flag is cleared

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
3	IPL1.3	IIC interrupt priority bit 1: IIC interrupt is high priority; 0: IIC interrupt is low priority

9.4. Secondary Bus Register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register1
0x50	IIC_FIL_MODE	RW	xxxx_xx10b	IIC filter selection register

9.4.1. External Port Function Selection Register 1

PERIPH_IO_SEL1 (34H) External port function selection register 1

Bit number	7	6	5	4
Symbol	UART1_IO_SEL	UART0_IO_SEL		IIC_IO_SEL

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1
Bit number	3	2	1	0
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INT0_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
4	IIC_IO_SEL	IIC port selection enable 0: Select IIC (SCL0B/SDA0B) function; 1: Select IIC (SCL0A/SDA0A) function

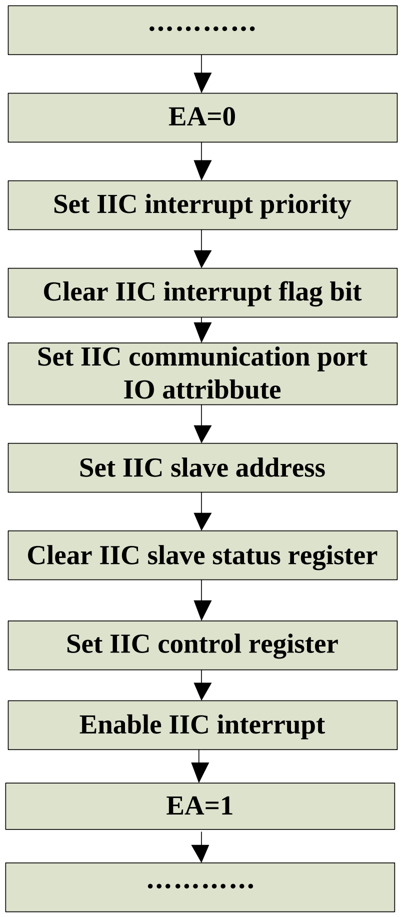
9.4.2. IIC Filter Selection Register

IIC_FIL_MODE (50H) IIC filter selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	IIC_AFIL_SEL	IIC_DFIL_SEL
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	1	0

Bit number	Bit symbol	Description
1	IIC_AFIL_SEL	IIC port analog filter selection enable 1: Select analog filter function; 0: Not select analog filter function;
0	IIC_DFIL_SEL	IIC port digital filter selection enable 1: Digital filter function is selected; 0: Digital filter function is not selected;

9.5. IIC Configuration Process



IIC configuration flow chart

Note: The IIC bus pull-up resistor is 4.7k~10k, and the filter capacitor to the ground is recommended to be 10pF~100pF close to the pin chip.

10. UART

There are 3 UART modules in the BF7515CM44-LJTX series. The BF7515CM44-LJTX provides the PERIPH_IO_SEL1 register. The Bit [6:5] of this register can control the selection of UART0 mapping IO port, and the Bit [7] of this register can control the selection of UART1 mapping IO port. Each module can only correspond to one set of mappings at the same time.

Features of UART interface in the system:

- Support full-duplex, half-duplex serial
- Independent dual buffer receiver and single buffer transmitter
- Programmed baud rate (10bit analog-to digital divider - Scalable to 12 digits)
- Interrupt-driven or polling operation:
  - send completed
  - receiving full
  - receive overflow, parity error, frame error
- Supports hardware parity production and check
- Programmable 8bit or 9bit character length
- STOP bit 1 or 2 can be selected
- Supports multiprocessor mode
- Support TXD/RXD pin position exchange
- Support TXD/RXD independent enable

10.1. UART Function Description

10.1.1. Baud Rate Generation

The baud rate generation modulus Baud_Mod is determined by the extension bit UART_BD_EXT.

UART_BD_EXT = 0, select the baud rate without expansion and maintain 10 bits: Baud_Mod = {UART _ BDH [1:0], UART _BDL}.

UART_BD_EXT = 1, select the baud rate to extend to 12 bits: Baud_Mod = {UART _ BD_ADD [1:0], UART_BDH[1:0], UART _BDL}.

Baud rate calculation formula: When Baud_Mod=0, the baud rate clock is not generated, when Baud_Mod>1, the baud rate = BUSCLK/(16xBaud_Mod). BUSCLK uses the frequency division clock of System clock source and is fixed at 24M. Each time the baud rate register is configured, the internal counter will be cleared to regenerate the baud rate signal. Communication requires that the transmitter and receiver use the same baud rate. The allowable baud rate deviation range for communication: 8/(11*16)=4.5%.

10.1.2. Transmitter Function

Send data flow: Trammitted by writing UART_BUF data, sending stop bit after sending stop bit. Software clear interrupt flag and waits for the next write. The transmitter output pin (TXD) idle state defaults to a logic high state. The entire transmission process must be performed when the module is enabled.

By writing data into the data register (UART_BUF), the data will be directly saved to the sending data buffer and the sending process will be started. In the subsequent complete sending process, the data buffer is locked, and the configuration write data register is invalid until the sending is completed after the stop bit, write UART_BUF again to restart a new transmission.

The central element of the serial port transmitter is the transmit shift register with a length of 10/11/12 bits (depending on the setting in the DATA_MODE control bit). Assuming DATA_MODE=0, select the normal 8-bit data mode. In 8-bit data mode, there are 1 start bit, 8 data bits, and 1/2 stop bits in the shift register.

Both sending and receiving are in little-endian mode (LSB first).

10.1.3. Receiver Function

The receiver is enabled by setting the RECEIVE_ENABLE bit in UART_CON1. Of course, the entire receiving process must be performed when the module is enabled.

Receiving data flow: When the receiving enable is valid, the data is received at any time, the receiving interrupt is set after receiving the stop bit, and the software clears the interrupt flag.

The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the flag. It is recommended that after detecting the receiving interrupt, read the status flag, read the data buf, and finally clear the received data status flag (UART_STATE[3:0]).

The data character is composed of a logic 0 start bit, 8 (or 9) data bits (LSB first) and a logic 1 stop bit (1bit). After receiving the stop bit into the receiving shifter, if the receiving data register is not full, the data character is transferred to the receiving data register, and the receiving data register is full status flag is set. If the receiving data register has been set to be full at this time, the overflow status flag is set, and the new data will be lost. Because the receiver is double-buffered, the program has a full character time for reading after setting the receive data register is full and before reading the data in the receive data buffer to avoid receiver overflow. When the program detects that the receive data register is full, it obtains data from the receive data register by reading UART_BUF.

10.1.4. Receiver Sampling Method

The receiver uses a 16 times baud rate clock for sampling. The receiver searches for the falling edge on the RXD serial data input pin by extracting logic level samples at 16 times the baud rate. The falling edge is defined as logic 0 samples after 3 consecutive logic 1 samples. The 16 times baud rate clock is used to divide the bit time into 16 segments, which are labeled RT1 to RT16.

The receiver then samples each bit time of RT8, RT9 and RT10, including the start bit and stop bit, to determine the logic level of the bit. The logic level is the logic level of the vast majority of samples taken during the bit time. When the falling edge is positioned, the logic level is 0 to ensure that this is the real start bit, not noise. If at least two of these three samples are 0, the receiver assumes that it is synchronized with the receiver character and starts Shift receives the following data, if the above conditions are not met, exit the state machine and return to the state of waiting for the falling edge.

The falling edge detection logic keeps looking for a falling edge. If an edge is detected, the sample clock resynchronizes the bit time. In this way, when noise or baud rate is not matched, the reliability of the receiver can be improved.

10.1.5. Multiprocessor Mode

In multi-processor mode, it only works in 9-bit mode. When the received R8 bit=1, the receive interrupt is set, otherwise it is not set. The function of this mechanism is to use hardware detection to eliminate the software overhead of processing unimportant information characters. Allow receivers to ignore characters in messages used for different receivers.

In this application system, all receivers estimate the Address character (bit 9 = 1) of each message. Once it is determined that the information is intended for different receivers, subsequent data characters (bit 9 = 0) will not be received.

Configuration process: Configure receiving enable, configure multiprocessor mode, receive Address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the Address matches, if it matches, the configuration closes the multiprocessor mode, and all subsequent data (The 9th bit = 0) can be received and interrupted, until the next Address data is received, the Address does not match, then the multi-processor mode is turned on, then all subsequent data will not be received, until the next Address data, in turn, loop application.

10.2. UART Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x98	UART2_STATE	R/RW	x000_0000b	UART2 status flag register
0xBA	UART2_BDL	RW	0000_0000b	UART2 baud rate control register
0xBB	UART2_CON1	RW	x000_0000b	UART2 mode control register 1
0xBC	UART_IO_CTRL1	RW	xx00_0000b	UART pin enable register
0xBD	UART2_BUF	RW	1111_1111b	UART2 port data register
0xC2	UART_IO_CTRL	RW	xxxx_x000b	UART TXD/RXD pin exchange register
0xD6	UART1_BDL	RW	0000_0000b	UART1 baud rate control register
0xD7	UART1_CON1	RW	x000_0000b	UART1 mode control register 1
0xD9	UART1_CON2	RW	xx00_1100b	UART1 mode control register 2
0xDA	UART1_STATE	RW	x000_0000b	UART1 status flag register
0xDB	UART1_BUF	RW	1111_1111b	UART1 port data register
0xDC	UART0_BDL	RW	0000_0000b	UART0 baud rate control register
0xDD	UART0_CON1	RW	x000_0000b	UART0 mode control register 1
0xDE	UART0_CON2	RW	xx00_1100b	UART0 mode control register 2
0xDF	UART0_STATE	RW	x000_0000b	UART0 status flag register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE2	UART0_BUF	RW	1111_1111b	UART0 port data register
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xED	UART2_CON2	RW	xx00_1100b	UART2 mode control register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

UART SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x34	PERIPH_IO_SEL1	RW	0001_0000b	External port function selection register 1
0x67	UART_BD_EXT	RW	xxxx_xxx0b	UART0/1/2 baud rate configuration extension bit register

UART secondary bus register list

10.3. UART0 Register

10.3.1. UART0 Status Flag Register

UART0_STATE (DFH) UART0 status flag register

Bit number	7	6	5	4
Symbol	-	UART0_R8	UART0_T8	TI0
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI0	UART0_RO	UART0_F	UART0_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	-	Reserved
6	UART0_R8	The 9th data of the receiver, read only
5	UART0_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI0	Send interrupt mark: 1: The sending buffer is empty 0: Send buffer is full, software write 0 to clear, write 1 is invalid
3	RI0	Receive interrupt mark: 1: The receive buffer is full 0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART0_RO	Receive overflow flag: 1: Receive overflow (new data is lost) 0: no overflow, software write 0 to clear, write 1 is invalid
1	UART0_F	Frame error flag: 1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART0_P	Parity error flag: 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

10.3.2. UART0 Baud Rate Control Register

UART0_BDL (DCH) UART0 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART0_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART0_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register UART_BD_EXT=0, Baud_Mod = {UART0_BDH[1:0], UART0_BDL}; UART_BD_EXT=1, Baud_Mod= {UART0_BD_ADD[1:0], UART0_BDH[1:0], UART0_BDL}; When Baud_Mod=0, the baud rate clock is not generated; When Baud_Mod>1, baud rate = BUSCLK/(16xBaud_Mod)

UART0_CON2 (DEH) UART0 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART0_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART0_BDH	
R/W	-	-	R/W	R/W	R/W		R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART0_BD_ADD	The upper 2 bits of the baud rate modulus divisor register (it is determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Send interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART0_BDH	The upper 2 bits of the baud rate modulus divisor register

10.3.3. UART0 Mode Control Register 1

UART0_CON1 (DDH) UART0 mode control register 1

Bit number	7	6	5	4

Symbol	-	UART0_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART0_ENABLE	Module enable 1: Module enable; 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on; 0: Receiver is off
4	MULTI_MODE	Multi-processor communication mode 1: Mode enable; 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled; 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check; 0: Even check

10.3.4. UART0 Port Data Register

UART0_BUF (E2H) UART0 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	--	Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

10.3.5. UART0 Pin Enable Register

UART_IO_CTRL1 (BCH) UART pin enable register

Bit number	7	6	5	4
Symbol	-	-	UART2_RXD_DIASB	UART2_TXD_DIASB
R/W	-	-	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
1	UART0_RXD_DIASB	UART0 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
0	UART0_TXD_DIASB	UART0 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled

10.3.6. UART0 TXD/RXD Pin Exchange

UART_IO_CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2	1	0
Symbol	-	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
0	UART0_PAD_CHANGE	UART0 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

10.4. UART1 Register

10.4.1. UART1 Status Flag Register

UART1_STATE (DAH) UART1 status flag register

Bit number	7	6	5	4
Symbol	-	UART1_R8	UART1_T8	TI1
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI1	UART1_RO	UART1_F	UART1_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_R8	Reserved
5	UART1_T8	The 9th data of the receiver, read only
4	TI1	The 9th data of the transmitter, read only when parity check is enabled
3	RI1	Send interrupt mark: 1: The sending buffer is empty; 0: Send buffer is full, software write 0 to clear, write 1 is invalid
2	UART1_RO	Receive interrupt mark 1: The receive buffer is full; 0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
1	UART1_F	Receive overflow flag 1: Receive overflow (new data is lost); 0: No overflow, software write 0 to clear, write 1 is invalid
0	UART1_P	Frame error flag 1: Frame error detected; 0: No frame error is detected, software writes 0 to clear, write 1 is invalid

10.4.2 UART1 Baud Rate Control Register

UART1_BDL (D6H) UART1 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART1_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART1_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register UART_BD_EXT=0, Baud_Mod = {UART1_BDH[1:0], UART1_BDL}; UART_BD_EXT=1, Baud_Mod= {UART1_BD_ADD[1:0], UART1_BDH[1:0], UART1_BDL}; When Baud_Mod=0, the baud rate clock is not generated; when Baud_Mod>1, baud rate = BUSCLK/(16xBaud_Mod)

UART1_CON2 (D9H) UART1 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART1_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART1_BDH	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART1_BD_ADD	The upper 2 bits of the baud rate modulus divisor register (It is determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Send interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
1~0	UART1_BDH	The upper 2 bits of the baud rate modulus divisor register

10.4.3. UART1 Mode Control Register 1

UART1_CON1 (D7H) UART1 mode control register 1

Bit number	7	6	5	4
Symbol	-	UART1_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART1_ENABLE	Module enable 1: Module enable; 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on; 0: Receiver is off
4	MULTI_MODE	Multi-processor communication mode 1: Mode enable; 0: Mode disable
3	STOP_MODE	Stop bit width selection; 1: 2 bits; 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode; 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled; 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check; 0: Even check

10.4.4 UART1 Port Data Register

UART1_BUF (DBH) UART1 port data register

Bit number	7	6	5	4	3	2	1	0

Symbol	-
R/W	R/W
Reset value	FF

Bit number	Bit symbol	Description
7~0	--	Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

10.4.5. UART1 Pin Enable Register

UART_IO_CTRL1 (BCH) UART pin enable register

Bit number	7	6	5	4
Symbol	-	-	UART2_RXD_DIASB	UART2_TXD_DIASB
R/W	-	-	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5	UART2_RXD_DIASB	UART2 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
4	UART2_TXD_DIASB	UART2 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled
3	UART1_RXD_DIASB	UART1 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
2	UART1_TXD_DIASB	UART1 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled

10.4.6. UART1 TXD/RXD Pin Exchange

UART_IO_CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2	1	0

Symbol	-	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
1	UART1_PAD_CHANGE	UART1 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

10.5. UART2 Register

10.5.1. UART2 Status Flag Register

UART2_STATE (98H) UART2 status flag register

Bit number	7	6	5	4
Symbol	-	UART2_R8	UART2_T8	TI2
R/W	-	R	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	RI2	UART2_RO	UART2_F	UART2_P
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART2_R8	The 9th data of the receiver, read only
5	UART2_T8	The 9th data of the transmitter, read only when parity check is enabled
4	TI2	Send interrupt mark: 1: The sending buffer is empty 0: Send buffer is full, software write 0 to clear, write 1 is invalid
3	RI2	Receive interrupt mark 1: The receive buffer is full 0: The receive buffer is empty, software writes 0 to clear, writes 1 is invalid
2	UART2_RO	Receive overflow flag 1: Receive overflow (new data is lost) 0: No overflow, software write 0 to clear, write 1 is invalid
1	UART2_F	Frame error flag

		1: Frame error detected 0: No frame error is detected, software writes 0 to clear, write 1 is invalid
0	UART2_P	Parity error flag 1: Receiver parity error 0: The parity check is correct, the software writes 0 to clear, and writes 1 is invalid

10.5.2. UART2 Baud Rate Control Register

UART2_BDL (BAH) UART2 baud rate control register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART2_BDL[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	UART2_BDL[7:0]	Baud rate control register, the lower 8 bits of the baud rate modulus divisor register UART_BD_EXT=0, Baud_Mod = {UART2_BDH[1:0], UART2_BDL}; UART_BD_EXT=1, Baud_Mod= {UART2_BD_ADD[1:0], UART2_BDH[1:0], UART2_BDL}; When Baud_Mod=0, the baud rate clock is not generated; when Baud_Mod>1, the baud rate = BUSCLK/(16xBaud_Mod)

UART2_CON2 (EDH) UART2 mode control register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	UART2_BD_ADD		TX_EMPTY_IE	RX_FULL_IE	UART2_BDH	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	
Reset value	-	-	0	0	1	1	0	0

Bit number	Bit symbol	Description
5~4	UART2_BD_ADD	The upper 2 bits of the baud rate modulus divisor register (It is determined by UART_BD_EXT whether to take effect)
3	TX_EMPTY_IE	Send interrupt enable 1: Interrupt enable; 0: Interrupt disable (used in polling mode)
2	RX_FULL_IE	Receive interrupt enable 1: Interrupt enable;

		0: Interrupt disable (used in polling mode)
1~0	UART2_BDH	The upper 2 bits of the baud rate modulus divisor register

10.5.3. UART2 Mode Control Register 1

UART2_CON1 (BBH) UART2 mode control register 1

Bit number	7	6	5	4
Symbol	-	UART2_ENABLE	RECEIVE_ENABLE	MULTI_MODE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	STOP_MODE	DATA_MODE	PARITY_EN	PARITY_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	UART2_ENABLE	Module enable 1: Module enable, 0: Module close
5	RECEIVE_ENABLE	Receiver enable 1: Receiver is on, 0: Receiver is off
4	MULTI_MODE	Multi-processor communication mode 1: Mode enable, 0: Mode disable
3	STOP_MODE	Stop bit width selection 1: 2 bits, 0: 1 bit
2	DATA_MODE	Data mode selection 1: 9-bit mode, 0: 8-bit mode
1	PARITY_EN	Parity check enable 1: Parity check is enabled, 0: Parity check is disabled
0	PARITY_SEL	Parity check selection 1: Odd check, 0: Even check

10.5.4 UART2 Port Data Register

UART2_BUF (BDH) UART2 port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	UART2_BUF[7:0]							
R/W	R/W							
Reset value	FF							

Bit number	Bit symbol	Description
7~0	UART2_BUF[7:0]	UART2 data register Read returns the contents of the read-only receive data buffer, write into the write-only transmit data buffer

10.5.5. UART2 Pin Enable Register

UART_IO_CTRL1 (BCH) UART Pin enable register

Bit number	7	6	5	4
Symbol	-	-	UART2_RXD_DIASB	UART2_TXD_DIASB
R/W	-	-	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	UART1_RXD_DIASB	UART1_TXD_DIASB	UART0_RXD_DIASB	UART0_TXD_DIASB
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
5	UART2_RXD_DIASB	UART2 RXD port disabled 0: RXD pin is enabled; 1: RXD pin is disabled
4	UART2_TXD_DIASB	UART2 TXD port disable 0: TXD pin is enabled; 1: TXD pin is disabled

10.5.6. UART2 TXD/RXD Pin Exchange

UART_IO_CTRL (C2H) UART TXD/RXD pin exchange register

Bit number	7~3	2	1	0
Symbol	-	UART2_PAD_CHANGE	UART1_PAD_CHANGE	UART0_PAD_CHANGE
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0

Bit number	Bit symbol	Description
2	UART2_PAD_CHANGE	UART2 TXD/RXD pin exchange 1: Pin exchange; 0: Pin not exchange

10.6. UART Interrupt Register

10.6.1. Interrupt Flag Register 2

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
3	IE11	UART1 interrupt flag 1: UART1 interrupt flag 0: Clear UART1 interrupt flag
2	IE10	UART0 interrupt flag 1: UART0 interrupt flag 0: Clear UART0 interrupt flag
0	IE8	UART2 interrupt flag 1:UART2 interrupt flag 0: Clear LVDT interrupt flag

10.6.2. Interrupt Enable Register 2

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
3	EX11	UART1 interrupt enable 1: UART1 interrupt enable; 0: UART1 interrupt disable
2	EX10	UART0 interrupt enable 1: UART0 enable; 0: UART0 disable
0	EX8	UART2 interrupt enable 1: UART2 interrupt enable; 0: UART2 interrupt disable

10.6.3. Interrupt Priority Register2

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
3	IPL2.3	UART1 priority selection bit. 1: UART1 interrupt is high priority; 0: UART1 interrupt is low priority
2	IPL2.2	UART0 priority selection bit. 1: UART0 interrupt is high priority; 0: UART0 interrupt is low priority
0	IPL2.0	UART2 priority selection bit. 1: UART2 interrupt is high priority; 0: UART2 interrupt is low priority

10.7. Secondary Bus Register

10.7.1. External Port Function Selection Register 1

PERIPH_IO_SEL1 (34H) External port function selection register 1

Bit number	7	6	5	4
Symbol	UART1_IO_SEL	UART0_IO_SEL		IIC_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1
Bit number	3	2	1	0
Symbol	INT3_IO_SEL	INT2_IO_SEL	INT1_IO_SEL	INT0_8_IO_SEL
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	UART1_IO_SEL	UART1 port selection enable 0: Select UART1 (RXD1B/TXD1B) function; 1: Select UART1 (RXD1A/TXD1A) function
6~5	UART0_IO_SEL	UART0 port selection enable 00: Select UART0 (RXD0C/TXD0C) function; 01: Select UART0 (RXD0A/TXD0A) function;

		1x: Select UART0 (RXD0B/TXD0B) function

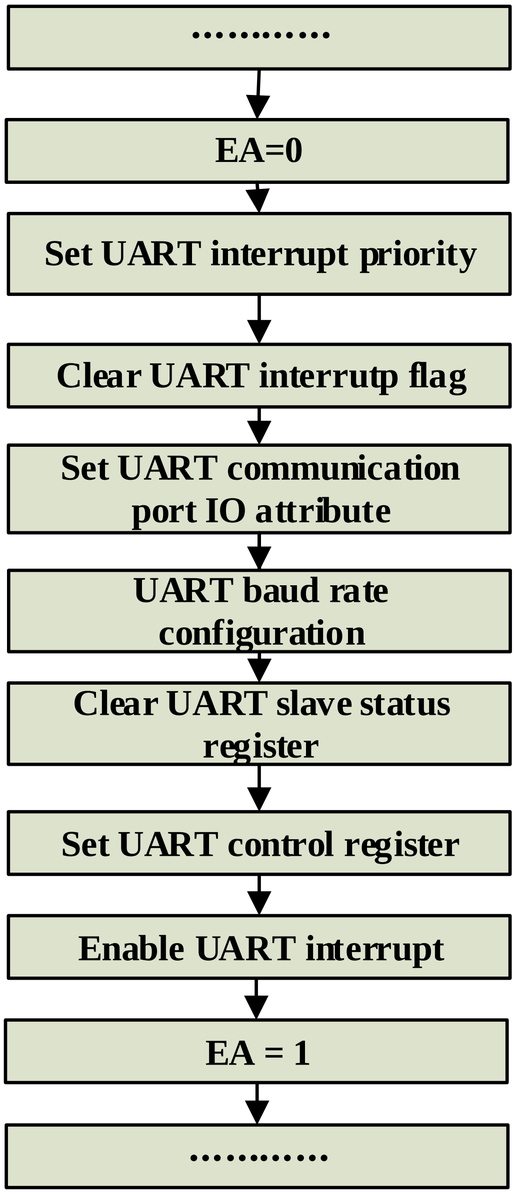
10.7.2. UART0/1/2 Baud Rate Configuration Extension Bit Register

UART_BD_EXT (67H) UART0/1/2 Baud rate configuration extension bit register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	UART0/1/2 baud rate configuration extension bit selection 1: Select the baud rate to extend to 12 bits; 0: Select the baud rate without extension to maintain 10 bits

10.8. UART Configure Process



UART initial configure process

Recommended application process:

1. Configuration module enable, receive enable, mode select: UART_CON1;
2. Configure baudrate, open interrupt enable: UART_BDL, UART_CON2;
3. Write UART_BUF to start sending data. After detecting the sending interrupt, clear the interrupt flag TI. Once the sending process is completed, wait for the next write to UART_BUF to start the sending process (it is not allowed to configure the next data in the sending process, including UART_BUF and UART_T8);
4. When the receiving interrupt is detected, first read the receiving status UART_STATE, then read R8 and UART_BUF, and finally clear the receiving status flag (UART_STAT [3:0] =

B0000). Once the receiving process is completed, wait for the next receiving interrupt.

5. If the configuration interrupt is not enabled and the program executes the UART function, it also needs to read the status flag first, then read R8 and UART_BUF, and finally clear the status flag.
6. Interrupt flag bit clearing operation. In full-duplex operation, the clear flag bit operation requires writing 0 for the effective interrupt bit and writing 1 for other interrupt bits (writing 1 is an invalid operation), otherwise it is easy to misuse. For example: when the transmission interrupt is valid, you need to write UART0_STATE = 0x0F; (that is, configure UART0_STATE 0:3] = 0x0F, and write R8 is invalid. When t8 is in 9-bit mode and no parity, you need to configure valid transmission data).
7. 8-bit mode: the parity check is disabled.
   9-bit mode: When the parity bit is enabled, when the ninth bit is not enabled, the ninth bit is UART_T8written in. There are only sending and receiving interrupts. The error flag only marks the error detection of the current data, and only the corresponding bit is cleared by writing 0. There is no error interrupt. The sending interrupt is set to 1 after the stop bit is sent, and the software is cleared to 0. The receiving interrupt is receiving Set to 1 after the stop bit is completed, cleared by software.

   Multi-processor mode: only work in 9-bit mode, when the received R8 bit = 1, the receive interrupt is set, otherwise it is not set. When using the multi-processor mode, configure the receive enable, configure the multi-processor mode, receive the address data (the 9th bit = 1), receive and generate an interrupt, the application confirms whether the address matches, and the configuration closes the multi-processor mode if it matches. Data (the 9th bit = 0) can be interrupted by the receive interrupt until the next address data is received. If the address does not match, the multi-processor mode is turned on, and all subsequent data will not be received until the next address data is cycled in turn application.

   Hardware response: Send data, start by writing UART_BUF value, set the sending interrupt flag after sending the stop bit, and clear the interrupt flag by software, and wait for the next write. When the receiving data is enabled, the data can be received at any time. After receiving the stop bit, the receiving interrupt is set and the software clears the interrupt flag. The currently received data will have a detection mechanism, which can detect three types of errors: receiving overflow, frame error, and parity error, all of which require software to clear the flag. It is recommended that after detecting the receiving interrupt, read the status flag and clear all the receiving status flags UART0/1_STATE [0:3].

11. SPI

SPI is a serial, synchronous, full/half duplex communication bus, the communication clock is 12MHz/8 MHz /4 MHz /1 MHz optional, the highest support 2MHz (master, slave) communication, the communication mode supports normal mode and high-speed mode. Four modes of clock idle level are selectable, SPI clock ratio is 50% (10% deviation allowed).

SPI normal mode: MCU writes SPI transmission buffer SPID through interrupt (when SPI enable is turned on, immediately generates a sending empty interrupt) or polling, the data is automatically loaded into the shift register, and sent to SPI_MOSI synchronously via SCLK; SPI_MISO receives data and loads it into the SPI receive buffer. When a receiving full interrupt is generated, the received data can be read from SPID.

SPI high-speed mode: MCU sends to SRAM to write and send data (up to 4K can be written). During communication, SPI reads the data to be sent directly from SRAM without interruption or polling; at the same time, every time a piece of data is received (8Bits), write the corresponding address of SRAM immediately. When the communication is completed, SPI generates a sending empty sign and a receiving full sign at the same time, and sends an interrupt.

Four modes of SFR configuration:

CPOL: Select clock idle state level:

0: The idle state of the clock is low;

1: Clock idle state is high level.

CPHA: Select the data moment of each cycle.

0: Data sampling is performed on the first transition edge (rising or falling edge) of the clock;

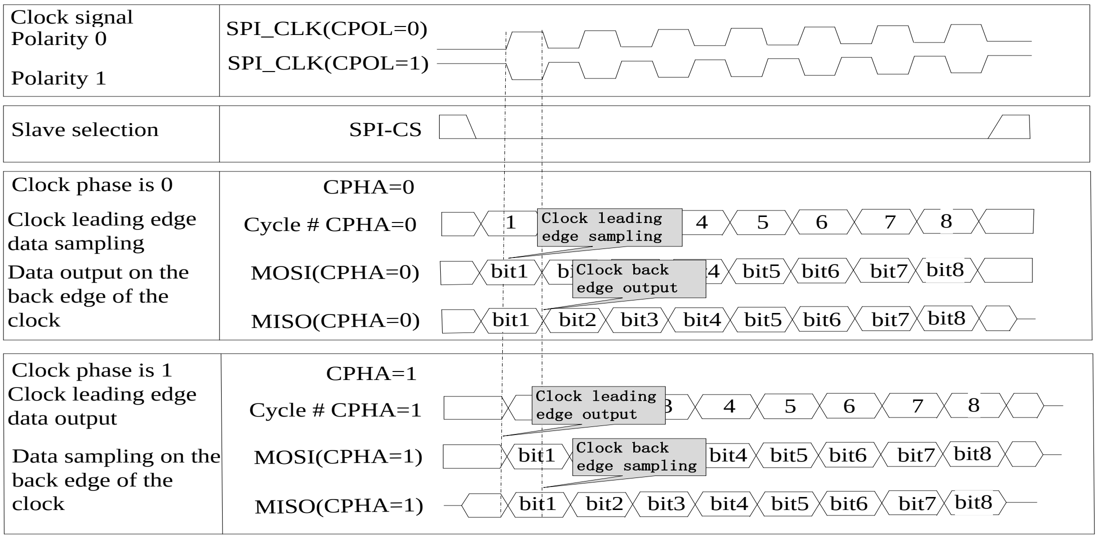
1: Data sampling is performed on the second transition edge (rising or falling edge) of the clock;

Mode 0 (CPOL=0, CPHA=0): The idle level of the clock is low, and the master and slave sample the data on the rising edge.

Mode 1 (CPOL=0, CPHA=1): The idle level of the clock is low, and the master and slave sample the data on the rising edge.

Mode 2 (CPOL=1, CPHA=0): The idle level of the clock is high, and the master and slave will sample the data on the rising edge.

Mode 3 (CPOL=1, CPHA=1): The clock idle level is high, and the master and slave machines sample data on the rising edge.



SPI working mode timing diagram

Description: SI: Slave sampling data; SO: Slave sending data; MI: Host sampling data; MO: Host sending data. PI_CS high level minimum time requirement is 1 SPI clock cycle.

11.1. SPI Port Configuration

To use the SPI function, you need to configure the relevant port as an SPI channel, and select the corresponding port input through the SPI communication port selection register. For example, configure PC0, PC1, PC2, and PC3 as SPI communication ports. Configure SPI_IO_SEL = 0x01:
SPI0B_CS: SPI chip select signal
SPI0B_CLK: SPI clock
SPI0B_MOSI: SPI master data output
SPI0B_MISO: SPI master data input

SPI_IO_SEL (68H) SPI communication port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	SPI_IO_SEL[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	SPI_IO_SEL[1:0]	SPI communication port selection register 01: PC2/3/4/5 selects SPI function 10: PE4/5/6/7 selects SPI function 00/11: PG0/1/2/3 selects SPI function

11.2. SPI Related Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xB5	SPI_CFG1	RW	0001_0101b	SPI configuration register1
0xB6	SPI_CFG2	RW	x001_1000b	SPI configuration register2
0xBE	SPI_STATE	RW	xxxx_x001b	SPI status register
0xBF	SPI_SPID	RW	0000_0000b	SPI cache operation register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

SPI SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x3E	SPI_TX_START_ADDR	RW	0000_0000b	SPI high-speed mode transmit buffer first address
0x3F	SPI_RX_START_ADDR	RW	0000_0000b	SPI high-speed mode receive buffer first address
0x40	SPI_NUM_L	RW	0000_0000b	SPI high-speed mode data buffer address number, low 8 bits
0x41	SPI_NUM_H	RW	xxxx_0000b	SPI high-speed mode data cache address number, high 4 bits
0x68	SPI_IO_SEL	RW	xxxx_xx00b	SPI communication port selection register
0x69	SPI_MCLK_MOD	RW	xxxx_xxx0b	SPI master mode receiver clock selection register

SPI Secondary bus register list

11.2.1. SPI Control Register 1

SPI_CFG1 (B5H) SPI control register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	RX_IE	SPI_EN	TX_IE	MSTR	CPOL	CPHA	LSBFE	CS_N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	1	0	1

Bit number	Bit symbol	Description
7	RX_IE	Receive enable- SPI receive buffer is full (SPRF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
6	SPI_EN	SPI enable: 1: module enable open; 0: module enable close
5	TX_IE	Transmit enable -SPI transmit buffer empty (SPTEF) interrupt enable 1: Interrupt is valid; 0: Interrupt is disabled (using polling)
4	MSTR	Master-slave mode selection 1: master mode; 0: slave mode
3	CPOL	SCLK active level selection 1: Active low; 0: Active high
2	CPHA	SCLK phase selection 1: Send data at the first valid clock edge 0: Sample data at the first valid clock edge
1	LSBFE	LSB first (shifter direction) 1: SPI serial data transmission starts from the lowest bit 0: SPI serial data transmission starts from the highest bit
0	CS_N	Chip select signal 0: Pull down CS; 1: Pull up CS

11.2.2. SPI Control Register 2

SPI_CFG2 (B6H) SPI control register 2

Bit number	7	6	5	4
Symbol	-	FEEDBACK	HSPEED_START	HALF_FUPLEX
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1
Bit number	3	2	1	0
Symbol	BIDIR_SELECT	SPR		

R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0

Bit number	Bit symbol	Description
6	FEEDBACK	Send the received data to the master\slave 1: Send the received data to the master\slave 0: Send the data written by MCU to the master\slave
5	HSPEED_START	The high-speed SPI communication mode is turned on and the hardware is automatically pulled down after the work is completed 1: High-speed SPI communication mode is on; 0: High-speed SPI communication mode is off In high-speed SPI mode, whether in slave or master mode, the chip select signal cannot be pulled high, which will cause the data sent by SPI to be lost
4	HALF_FUPLEX	Half-duplex mode selection: 1: Select half-duplex mode; 0: Select full-duplex mode
3	BIDIR_SELECT	Half-duplex mode, transmission and reception direction selection 1: Send; 0: Seceive
2~0	SPR	SPI baud rate coefficient: maximum communication frequency 2MHz 000: spi_clk/2; 001: spi_clk /4; 010: spi_clk/6; 011: spi_clk /8; 100: spi_clk/10; 101: spi_clk /12; 110: spi_clk/14; 111: spi_clk /16;

11.2.3. SPI Status Flag Register

SPI_STATE (BEH) SPI status flag register

Bit number	7~3	2	1	0
Symbol	-	SPRF	OVERFLOW_RX	SPTEF
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	1

Bit number	Bit symbol	Description
7~3	--	Reserved
2	SPRF	Read buffer full mark, software write 0 to clear 0: No data is available in the receive data buffer; 1: There is data in the receive data buffer

1	OVERFLOW_RX	In the normal communication mode, when the receiving overflow is caused by not reading in time, OVERFLOW_RX=1, the signal does not generate an interrupt, only the mark In high-speed SPI communication mode, it is invalid (when the number of received data is equal to the configured {SPI_NUM_H, SPI_NUM_L}, the work will end, SPRF will be set, and a full interrupt will be generated).
0	SPTEF	Send buffer empty mark, write into SPID hardware to clear automatically. In the SPI idle state, the first data written to SPID will be directly stored in the shift register, and the second data written will be loaded into the transmit buffer, and SPTEF will be automatically pulled low. 1: The data buffer is empty and data can be written; 0: The data buffer is not empty

11.2.4. SPI Port Data Register

SPI_SPID (BFH) SPI port data register

Bit number	7	6	5	4	3	2	1	0
Symbol	SPI_SPID[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPI_SPID[7:0]	SPID reading this register will return the data read from the receive data buffer rx_reg. Writing to this register will write data into the transmit data buffer tx_reg. Data should not be written into the transmit data buffer, unless the SPI transmit buffer empty flag (SPTEF) is set, indicating that there is a certain space in the transmit buffer to queue new transmit bytes. After setting the SPRF and before completing another transmission, you can read data from the SPID at any time. If the data is not read from the receive data buffer before the end of the new transmission, the receive overflow will result and the newly transmitted data will be lost.

11.2.5. SPI Interrupt Register

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
5	IE13	SPI interrupt flag 1: With SPI interrupt flag 0: Clear SPI interrupt flag

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
5	EX13	SPI interrupt enable 1: SPI interrupt enable; 0: SPI interrupt disable

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
5	IPL2.5	SPI priority selection bit. 1: SPI priority is high; 0: SPI priority is low

11.3. SPI Secondary Bus Register

11.3.1. SPI High-speed Mode Transmit Buffer First Address

SPI_TX_START_ADDR (3EH) SPI high speed mode transmit buffer first address

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description

7~0	--	In SPI high-speed mode, the first address of the transmit data buffer, SPI_TX_START_ADDR*16

11.3.2. SPI High-speed Mode Receiving Buffer First Address

SPI_RX_START_ADDR (3FH) SPI High-speed mode receiving buffer first address

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In SPI high-speed mode, the first address of the receive data buffer, SPI_RX_START_ADDR*16

11.3.3. SPI Number of Data Cache Addresses in High-speed Mode

SPI_NUM_L (40H) SPI high-speed mode data buffer address number low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPI_NUM_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPI_NUM_L[7:0]	Number of data buffer addresses in SPI high-speed mode, low 8 bits

SPI_NUM_H (41H) SPI high-speed mode data cache address number, high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SPI_NUM_H [3:0]			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	SPI_NUM_H[3:0]	Number of data buffer addresses in SPI high-speed mode, high 4 bits

11.3.4. SPI Communication Port selection Register

SPI_IO_SEL (68H) SPI communication port selection register

Bit number	7	6	5	4	3	2	1	0

Symbol	-	-	-	-	-	-	SPI_IO_SEL[1:0]	
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1~0	SPI_IO_SEL[1:0]	SPI communication port selection register 01: PC2/3/4/5 selects SPI function 10: PE4/5/6/7 selects SPI function 00/11: PG0/1/2/3 selects SPI function

11.3.5. SPI Master Mode Receiver Clock Selection Register

SPI_MCLK_MOD (69H) SPI master mode receiver clock selection register

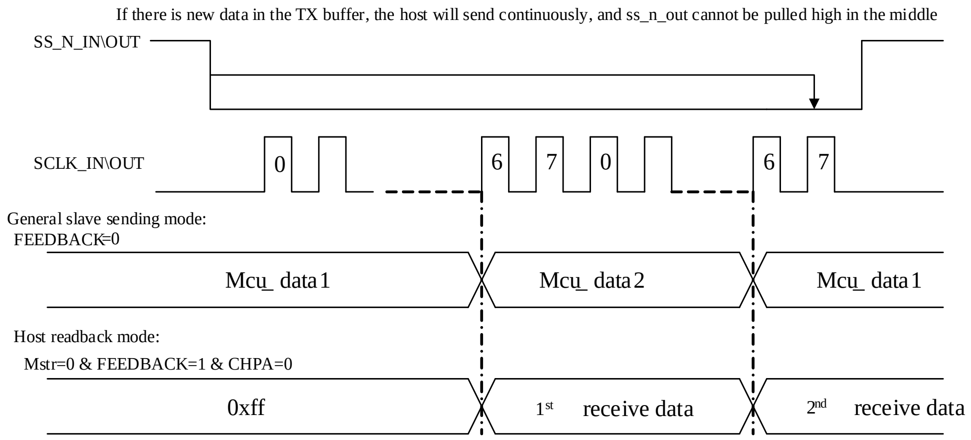
Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	SPI master mode receiver clock selection register 1: Select the host output as the receive clock; 0: Select the PAD port input as the receive clock

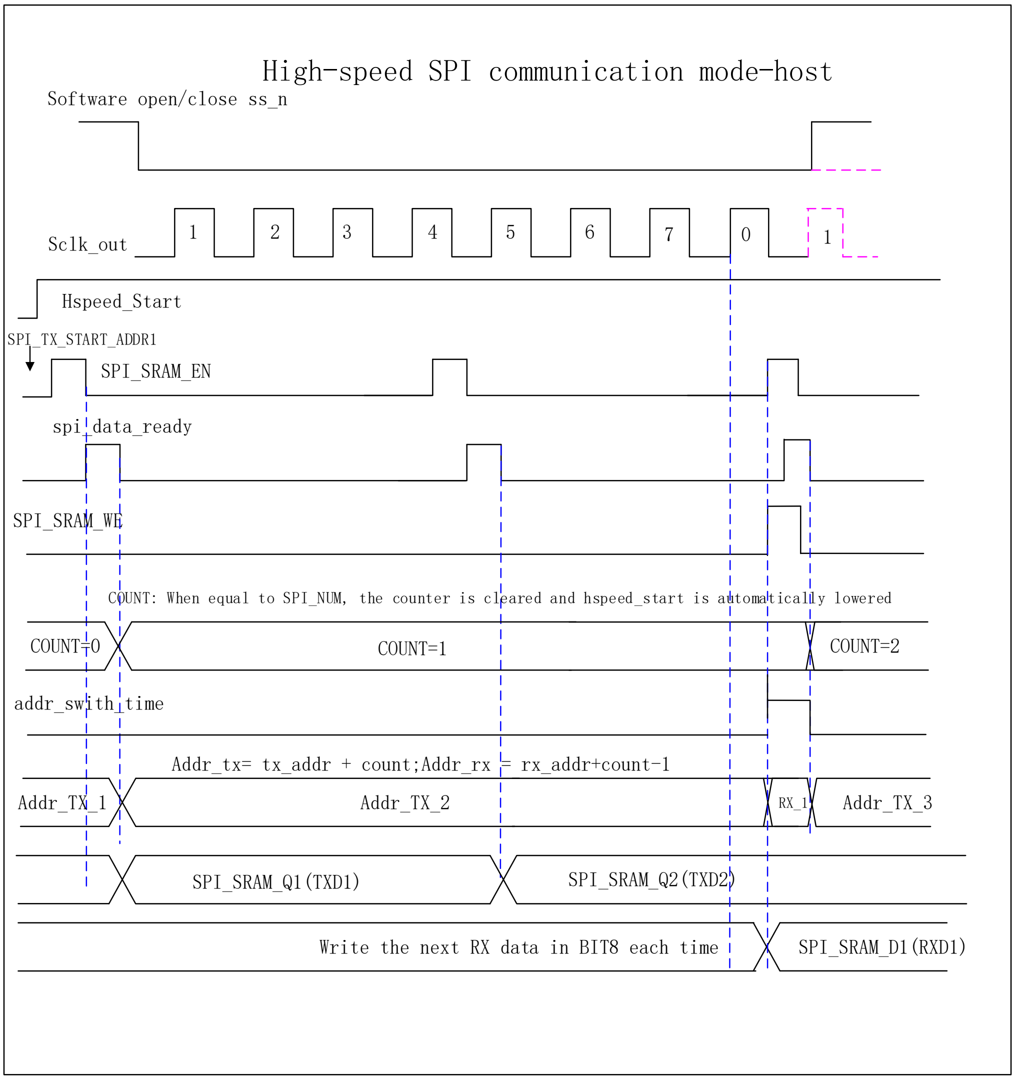
11.4. Communication Timing

There are three flag bits, two interrupt mask bits and an interrupt vector related to the SPI system. The SPI receive interrupt enable bit (RX_IE) allows interrupts from the SPI receiver full flag (SPRF) to occur. The SPI transmit interrupt enable bit (TX_IE) allows interrupts from the SPI transmit buffer empty flag (SPTIEF) to occur. When a flag bit is set and the related interrupt enable bit is set, the hardware interrupt request is sent to the CPU. If the interrupt enable bit is cleared, the software can poll the relevant flag bit without interruption. The SPI interrupt service routine (ISR) should check the flag bit to determine the event that caused the interrupt. Before returning from the ISR (usually near the starting point of the ISR), the service program should also clear the flag bit.

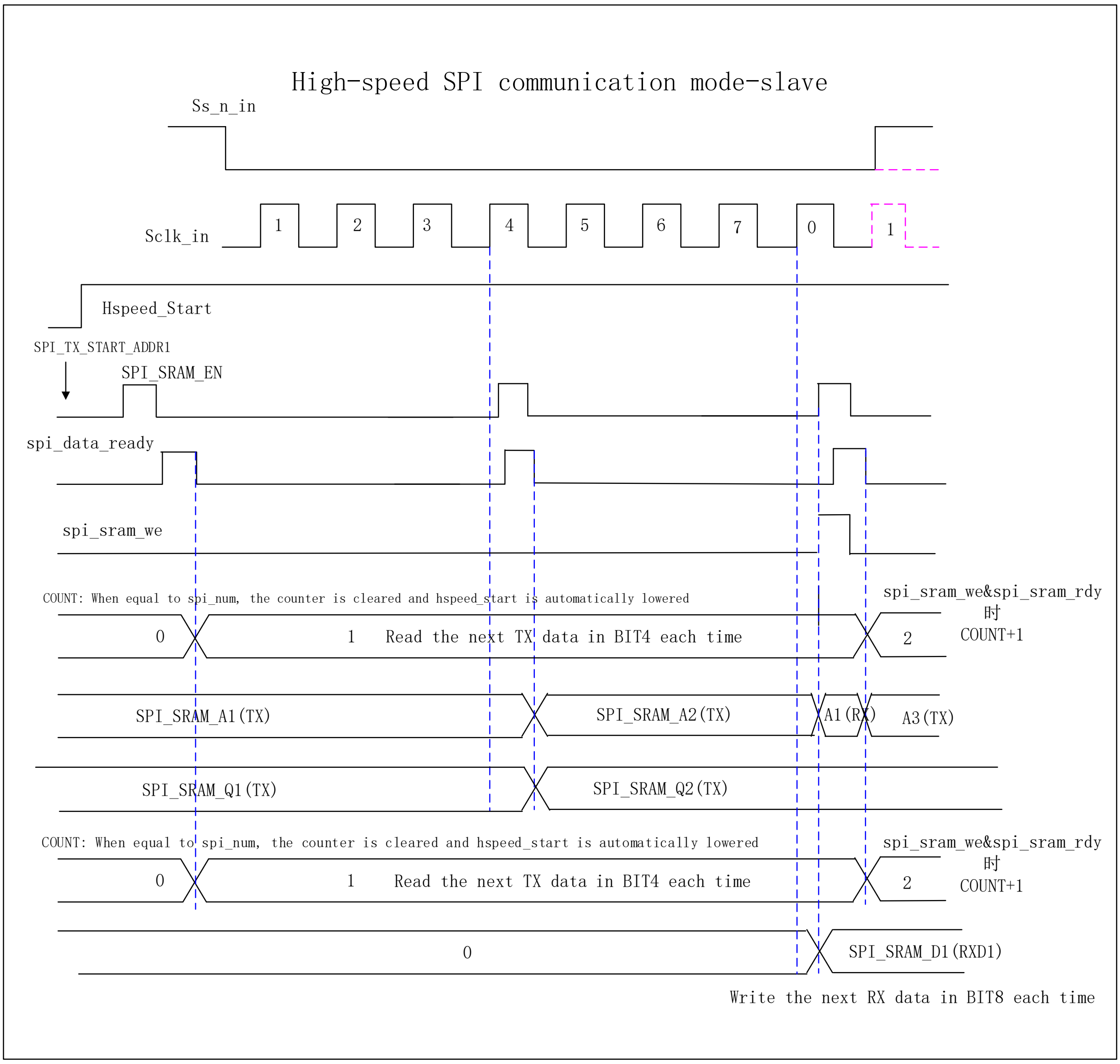
Schematic diagram of SPI continuous working in normal communication mode:



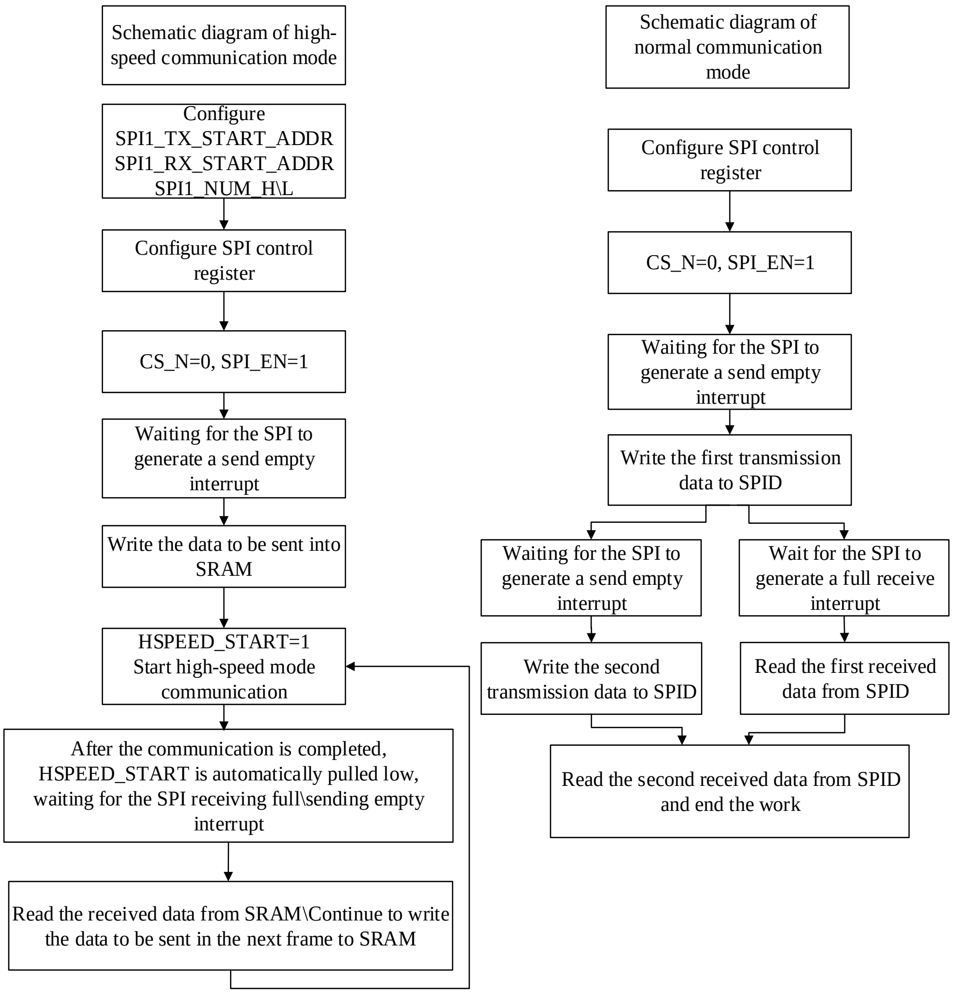
Schematic diagram of SPI continuous working in high-speed communication mode (host):



Schematic diagram of SPI continuous working in high-speed communication mode (slave):



11.5. SPI Configuration Process



SPI workflow diagram

Note:

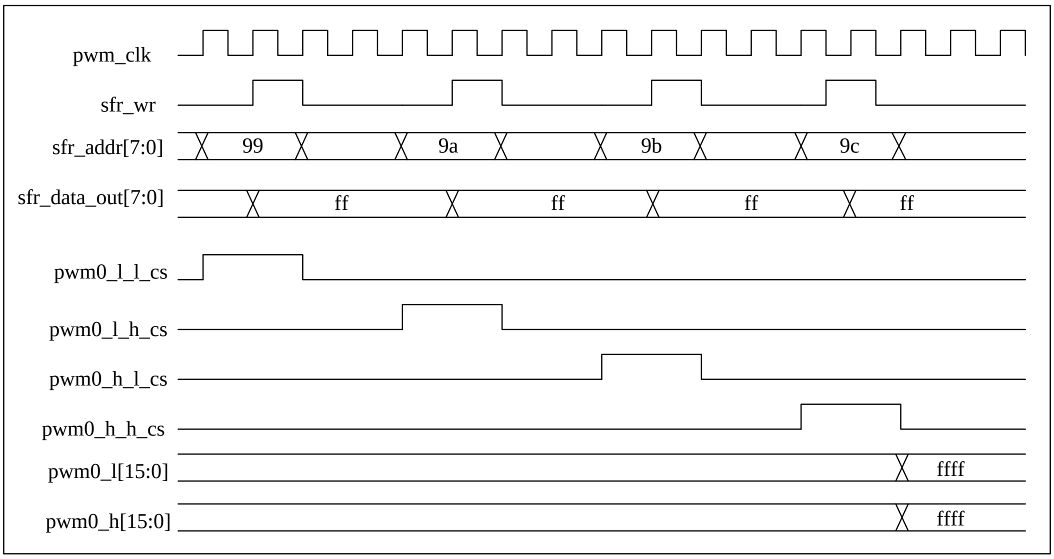
1. Configure CPOL and CPHA when the chip selection is high, otherwise SCLK has glitches (master, slave)
2. In high-speed mode, hspeed start will be automatically pulled low after the work is completed. At this time, the host can no longer send SCLK, otherwise an unstable state will occur.
3. In slave mode, after the chip select is pulled low, SPI_EN cannot be turned off. Otherwise, when the SPI EN is reopened, when the chip select becomes low again, the internally **gene**rated SCLK will have a glitch. That is, while SPI is selected, SPI_EN cannot be turned off.
4. In the slave mode, if the chip select is always 0, if you need to switch CPOL\CPHA\LSBFE midway, the slave can only switch after the master raises the chip select.
5. In high-speed mode, if an odd number of data is sent in each frame, the chip select signal needs to be pulled up once between each frame.

12. PWM

The functional characteristics of PWM are as follows:

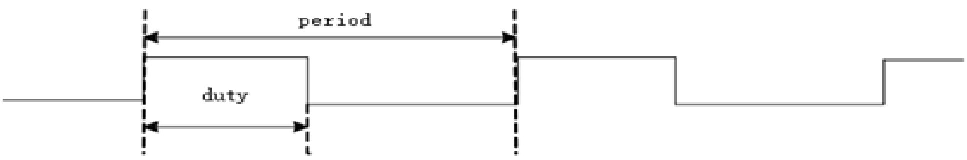
- 4 independent PWM modules;
- high-level control register and low-level control register: 16-bit register;
- Output period: Tpwm_data = (PWM_H + PWM_L) *Tpwm_clk;
- Output duty cycle: Dpwm_data = PWM_H/ (PWM_L + PWM_H);
- PWM 0 shares period and duty cycle, each channel has independent polarity control;
- PWM 1 shares period and duty cycle, each channel has independent polarity control;
- PWM 2 and PWM 3 each support one output port and the polarity is not selectable
- PWM 0 and PWM 1 can be configured to output overflow interrupt respectively, PWM2 and PWM 3 do not support;
- Support common frequency: 38kHz (infrared application)

When the PWM 0 and PWM 1 count values are full, an overflow interrupt occurs, and the interrupt enable configuration is valid, the core enters the PWM interrupt.



The period and pulse width of the PWM pulse width modulation module can be configured through registers. When PWM_H + PWM_L = 0, the output is low, but the configuration of the register must be selected when the PWM output port is valid (active high) and high The high level control register and the low level control register must be configured in order from low to high, in order to ensure that the internal counter of the PWM module counts correctly and avoid generating wrong waveforms.

PWM waveform intent



12.1. PWM Channel Configuration

The BF7515CM44-LJTX provide 4 independent 16bit PWM modules.

- PWM 0 supports 5 output ports (PWM0A, PWM0B, PWM0C, PWM0D, PWM0E);
- PWM 1 supports 5 output ports (PWM1A, PWM1B, PWM1C, PWM1D, PWM1E);
- PWM 2 supports 1 output ports (PWM 2);
- PWM 3 supports 1 output ports (PWM 3);

PWM0 and PWM1 of the BF7515CM44-LJTX provide 8 output channels at most. When PWM0A and PWM1E are configured at the same time, PWM0A is valid and PWM1E is invalid; when PWM0B and PWM1D are configured at the same time, PWM0B is valid and PWM1D is invalid. See PWM port selection register (PWM_IO_SEL) and PWM port selection register 1 (PWM_IO_SEL1).

12.2. PWM Related Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0x99	PWM0_L_L	RW	0000_0000b	PWM0 low level control register(low 8-bit)
0x9A	PWM0_L_H	RW	0000_0000b	PWM0 low level control register (high 8-bit)
0x9B	PWM0_H_L	RW	0000_0000b	PWM0 high level control register(low 8-bit)
0x9C	PWM0_H_H	RW	0000_0000b	PWM0 high level control register (high 8-bit)
0x9D	PWM1_L_L	RW	0000_0000b	PWM1 low level control register(low 8-bit)
0x9E	PWM1_L_H	RW	0000_0000b	PWM1 low level control register (high 8-bit)
0x9F	PWM1_H_L	RW	0000_0000b	PWM1 high level control register(low 8-bit)
0xA1	PWM1_H_H	RW	0000_0000b	PWM1 high level control register (high 8-bit)
0xA2	PWM2_L_L	RW	0000_0000b	PWM2 low level control register(low 8-bit)
0xA3	PWM2_L_H	RW	0000_0000b	PWM2 low level control register (high 8-bit)
0xA4	PWM2_H_L	RW	0000_0000b	PWM2 high level control register(low 8-bit)
0xA5	PWM2_H_H	RW	0000_0000b	PWM2 high level control register (high 8-bit)
0xA6	PWM3_L_L	RW	0000_0000b	PWM3 low level control register(low 8-bit)
0xA7	PWM3_L_H	RW	0000_0000b	PWM3 low level control register (high 8-bit)
0xA9	PWM3_H_L	RW	0000_0000b	PWM3 high level control register(low 8-bit)
0xAA	PWM3_H_H	RW	0000_0000b	PWM3 high level control register (high 8-bit)
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1
0xFA	PWM_INT_CTRL	RW	xxxx_xx00b	PWM interrupt enable control register

12.2.1. PWM0 Level Control Register

PWM0_L_L (99H) PWM0 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_L_H (9AH) PWM0 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_H_L (9BH) PWM0 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM0_H_H (9CH) PWM0 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

12.2.2. PWM1 Level Control Register

PWM1_L_L (9DH) PWM1 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_L_H (9EH) PWM1 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_H_L (9FH) PWM1 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

PWM1_H_H (A1H) PWM1 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM1_H_H [7:0]							
R/W	R/W							
Reset value	0							

12.2.3. PWM2 Level Control Register

PWM2_L_L (A2H) PWM2 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_L [7:0]							
R/W	R/W							
Reset value	0							

PWM2_L_H (A3H) PWM2 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_L_H [7:0]							
R/W	R/W							
Reset value	0							

PWM2_H_L (A4H) PWM2 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM2_H_H (A5H) PWM2 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM2_H_H [7:0]							
R/W	R/W							
Reset value	0							

12.2.4. PWM3 Level Control Register

PWM3_L_L (A6H) PWM3 low level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM3_L_L [7:0]							
R/W	R/W							
Reset value	0							

PWM3_L_H (A7H) PWM3 low level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM3_L_H [7:0]							
R/W	R/W							
Reset value	0							

PWM3_H_L (A9H) PWM3 high level control register (low 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM3_H_L [7:0]							
R/W	R/W							
Reset value	0							

PWM3_H_H (AAH) PWM3 high level control register (high 8-bit)

Bit number	7	6	5	4	3	2	1	0
Symbol	PWM3_H_H[7:0]							
R/W	R/W							
Reset value	0							

12.2.5. PWM0 and PWM1 Interrupt Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
7	INT_PWM1_STAT	PWM1 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM1 channel 1: Interrupt is valid; 0: Interrupt is invalid
2	INT_PWM0_STAT	PWM0 interrupt status flag, this bit is cleared by writing 0, and it can also be cleared by closing the PWM0 channel 1: Interrupt is valid; 0: Interrupt is invalid

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
4	IE12	Timer3/PWM1 interrupt flag 1: Timer3/PWM1 interrupt flag 0: Clear Timer3/PWM1 interrupt flag

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	EX7	WDT/Timer2/PWM0 interrupt enable 1: WDT/Timer2/PWM0 interrupt enable; 0: WDT/Timer2/PWM0 interrupt disable

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
4	EX12	Timer3/PWM1 interrupt enable 1: Timer3/PWM1 interrupt enable; 0: Timer3/PWM1 interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IE7	WDT/Timer2/PWM0 interrupt flag 1: With interrupt flag; 0: Without interrupt flag

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
4	IPL2.4	Timer3/PWM1 priority selection bit 1: Timer3/PWM1 interrupt is high priority; 0: Timer3/PWM1 interrupt is low priority

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
7	IPL1.7	WDT/Timer 2/PWM0 interrupt priority bit 1: WDT/Timer 2/PWM0 interrupt is high priority; 0: WDT/Timer 2/PWM0 interrupt is low priority

PWM_INT_CTRL (FAH) PWM interrupt enable control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	--	PWM1 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disable
0	--	PWM0 counter overflow interrupt 1: Interrupt enable; 0: Interrupt disabled

12.3. Secondary Bus Register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x33	PWM_IO_SEL	RW	0000_0000b	PWM port selection register
0x59	PWM_IO_SEL1	RW	xxxx_0000b	PWM port selection register 1
0x60	PWM0_POLA_SEL	RW	xxx0_0000b	PWM0 polarity selection register
0x61	PWM1_POLA_SEL	RW	xxx0_0000b	PWM1 polarity selection register

12.3.1. PWM Port Selection Register

PWM_IO_SEL (33H) PWM port selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	PWM_IO_SEL[7]	PWM3 selection enable 1: PWM3 function is selected; 0: PWM3 function is not selected
6	PWM_IO_SEL[6]	PWM2 selection enable 1: PWM2 function is selected; 0: PWM2 function is not selected
5	PWM_IO_SEL[5]	PWM1C selection enable 1: PWM1C function is selected; 0: PWM1C function is not selected
4	PWM_IO_SEL[4]	PWM1B selection enable 1: PWM1B function is selected; 0: PWM1B function is not selected
3	PWM_IO_SEL[3]	PWM1A selection enable 1: PWM1A function is selected; 0: PWM1A function is not selected
2	PWM_IO_SEL[2]	PWM0C selection enable 1: PWM0C function is selected; 0: PWM0C function is not selected
1	PWM_IO_SEL[1]	PWM0B selection enable 1: PWM0B function is selected; 0: PWM0B function is not selected When PWM0B and PWM1D are configured at the same time, PWM0B is valid and PWM1D is invalid
0	PWM_IO_SEL[0]	PWM0A selection enable 1: PWM0A function is selected; 0: PWM0A function is not selected When PWM0A and PWM1E are configured at the same time, PWM0A is valid and PWM1E is invalid

12.3.2. PWM Port Selection Register 1

PWM_IO_SEL1 (59H) PWM port selection register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3	PWM_IO_SEL[3]	PWM1E selection enable 1: PWM1E function is selected; 0: PWM1E function is not selected When PWM1E and PWM0A are configured at the same time, PWM0A is valid and PWM1E is invalid
2	PWM_IO_SEL[2]	PWM1D selection enable 1: PWM1D function is selected; 0: PWM1D function is not selected When PWM1D and PWM0B are configured at the same time, PWM0B is valid and PWM1D is invalid
1	PWM_IO_SEL[1]	PWM0E selection enable 1: PWM0E function is selected; 0: PWM0E function is not selected
0	PWM_IO_SEL[0]	PWM0D selection enable 1: PWM0D function is selected; 0: PWM0D function is not selected

12.3.3. PWM0 Polarity Selection Register

PWM0_POLA_SEL (60H) PWM0 polarity selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
7~5	--	Reserved
4	--	PWM0E output polarity selection 1: Reverse output; 0: Normal output
3	--	PWM0D output polarity selection 1: Reverse output; 0: Normal output
2	--	PWM0C output polarity selection 1: Reverse output; 0: Normal output
1	--	PWM0B output polarity selection 1: Reverse output; 0: Normal output

0	--	PWM0A output polarity selection 1: Reverse output; 0: Normal output

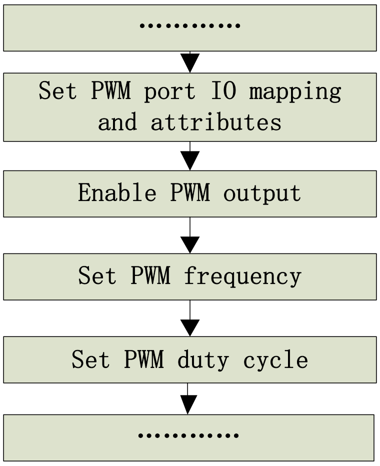
12.3.4. PWM1 Polarity Selection Register

PWM1_POLA_SEL (61H) PWM1 polarity selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset value	-	-	-	0	0	0	0	0

Bit number	Bit symbol	Description
7~5	--	Reserved
4	--	PWM1E output polarity selection 1: Reverse output; 0: Normal output
3	--	PWM1D output polarity selection 1: Reverse output; 0: Normal output
2	--	PWM1C output polarity selection 1: Reverse output; 0: Normal output
1	--	PWM1B output polarity selection 1: Reverse output; 0: Normal output
0	--	PWM1A output polarity selection 1: Reverse output; 0: Normal output

12.4. PWM Configuration Process



PWM Schematic diagram of configuration process

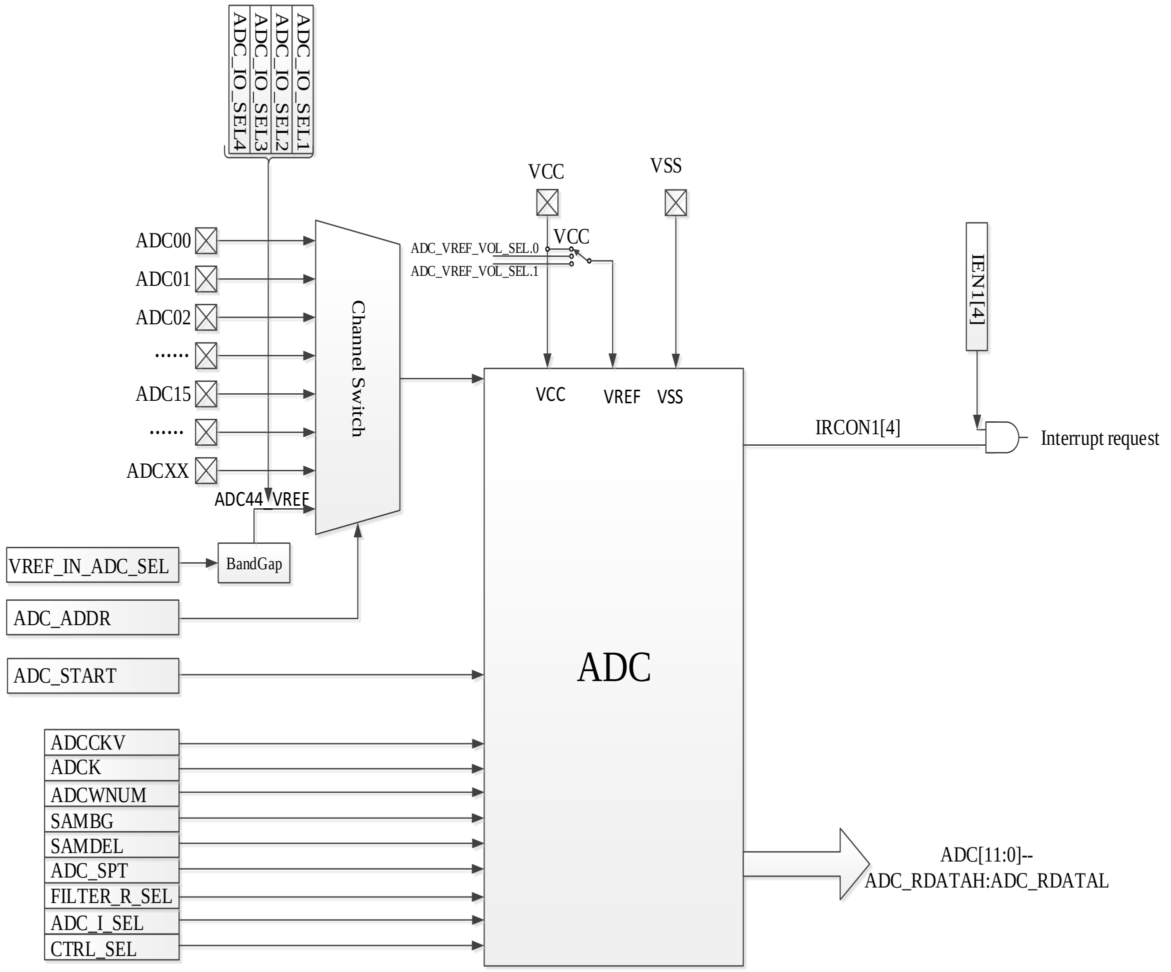
Note: frequency range: 184Hz ~ 120kHz recommended.

13. ADC

The BF7515CM44-LJTX chip contains a single-ended, 12-bit linear successive approximation analog-to-digital converter (ADC), and the reference voltage of the ADC is connected to the VCC of the chip. ADC channels can input independent analog signals. The ADC module converts 1 channel each time, ADC_START=0→1(rising edge) starts the conversion, after the conversion is completed, the ADC result register is updated and an interrupt is generated.

The BF7515CM44-LJTX chip has the following characteristics:

- 12-bit resolution linear and successive approximation to ADC
- Single conversion mode
- Sampling time and conversion speed can be configured
- Support wake up in idle mode 0



ADC structure block diagram

13.1. ADC Related Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xC1	ADC_SPT	RW	0000_0000b	ADC sampling time configure register
0xC3	ADC_SCAN_CFG	RW	x000_0000b	ADC scan configuration register
0xC4	ADCCKC	RW	0000_0000b	ADC clock and filter configuration register
0xC5	ADC_RDATAH	R	xxxx_0000b	ADC scan result register, high 4 bits
0xC6	ADC_RDATAL	R	0000_0000b	ADC scan result register, low 8 bits
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

ADC SFR register list

Secondary bus register				
Addr	**Name**	**RW**	**Reset**	**Description**
0x2A	ADC_IO_SEL0	RW	x000_0000b	ADC function selection register 0
0x2D	PD_ANA	RW	x111_xx11b	Analog ADC judgment register
0x32	ADC_CFG_SEL	RW	x000_0000b	ADC configuration register
0x42	ADC_CFG_SEL1	RW	xx00_0010b	ADC comparator offset cancellation selection register
0x53	ADC_IO_SEL1	RW	0000_0000b	ADC select enable register 1
0x54	ADC_IO_SEL2	RW	0000_0000b	ADC select enable register 2
0x55	ADC_IO_SEL3	RW	0000_0000b	ADC select enable register 3
0x56	ADC_IO_SEL4	RW	0000_0000b	ADC select enable register 4
0x57	ADC_IO_SEL5	RW	xxx0_0000b	ADC select enable register 5

ADC list of secondary bus registers

13.1.1. ADC Sampling Time Configuration Register

ADC_SPT (C1H) ADC sample time configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_SPT[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_SPT[7:0]	ADC sampling time configuration register Sampling time: t1= (ADC_SPT+1)*4* T_{ADCK}

13.1.2. ADC Scan Configuration Register

ADC_SCAN_CFG (C3H) ADC scan configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADC_ADDR						ADC_START
R/W	-	R/W						R/W
Reset value	-	0						0

Bit number	Bit symbol	Description
6~1	ADC_ADDR	ADC channel address selection register 000000: corresponding to ADC0; 000001: corresponding to ADC1; …… 101010: corresponding to ADC42; 101011: corresponding to ADC43; 101100: corresponding to ADC44_VREF Other: Reserved
0	ADC_START	ADC scan open register 0: ADC module does not scan; 1: ADC module starts to scan ADC_START is set from 0 to 1, ADC starts to scan, after one scan, ADC_START hardware is automatically set to 0, corresponding to the ADC interrupt flag bit, the ADC interrupt flag bit needs to be cleared by software Note: ADC_START is not allowed to be configured during scanning

13.1.3. ADC Clock and Filter Configuration Register

ADCCKC (C4H) ADC clock and filter configuration register

Bit number	7	6	5	4
Symbol	FILTER_SEL	SAMBG	SAMDEL	
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	ADCCKV		ADCK	
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description

7	FILTER_SEL	ADC input signal filter selection 0: No RC filter added; 1: RC filter added.
6	SAMBG	Sampling timing and comparison timing interval selection 0: interval of 0 T_{ADCK}; 1: interval of 1 T_{ADCK}
5~4	SAMDEL	Sampling delay time selection 00: 0*T_{ADCK}; 01: 2*T_{ADCK}; 10: 4*T_{ADCK}; 11: 8*T_{ADCK}
3~2	ADCCKV	ADC comparator offset cancellation analog input clock 00: 12MHz; 01: 8MHz; 10: 4MHz; 11: 2MHz
1~0	ADCK	ADC clock 00: 8MHz; 01: 6MHz; 10: 4MHz; 11: 3MHz

13.1.4. ADC Scan Result Register

ADC_RDATAH (C5H) ADC scan result register high 4 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ADC_RDATAH [3:0]			
R/W	-	-	-	-	R			
Reset value	-	-	-	-	0			

ADC_RDATAL (C6H) ADC scan result register, low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_RDATAL[7:0]							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
3~0	ADC_RDATAH[3:0]	ADC scan result register
7~0	ADC_RDATAL[7:0]	ADC scan result register

13.1.5. ADC Interrupt Register

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
4	EX4	ADC interrupt enable

		1: ADC interrupt enable; 0: ADC interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
4	IE4	ADC interrupt flag 1: ADC interrupt flag is present; 0: ADC interrupt flag is cleared

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
4	IPL1.4	ADC interrupt priority 0: ADC is low priority; 1: ADC is high priority

13.2. ADC Secondary Bus Register

13.2.1. ADC Function Selection Register

ADC_IO_SEL0 (2AH) ADC function selection register 0

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADC_IO_SEL0 [6:0]						
R/W	-	R/W						
Reset value	-	0						

Bit number	Bit symbol	Description
6~0	ADC_IO_SEL0[6:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 0000001=ADC0; 0000010=ADC1; 0000100=ADC2; 0001000=ADC3; 0010000=ADC4; 0100000=ADC5;

		1000000=ADC6

ADC_IO_SEL1 (53H) ADC select enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL1 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL1 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC7; 00000010=ADC8; 00000100=ADC9; 00001000=ADC10; 00010000=ADC11; 00100000=ADC12; 01000000=ADC13; 10000000=ADC14

ADC_IO_SEL2 (54H) ADC select enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL2 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL2 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC15; 00000010=ADC16; 00000100=ADC17; 00001000=ADC18; 00010000=ADC19; 00100000=ADC20; 01000000=ADC21; 10000000=ADC22

ADC_IO_SEL3 (55H) ADC select enable register 3

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL3[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL3 [7:0]	Enable the ADC control function that disables analog input pins

		1: Select ADC function; 0: Not select ADC function 00000001=ADC23; 00000010=ADC24; 00000100=ADC25; 00001000=ADC26; 00010000=ADC27; 00100000=ADC28; 01000000=ADC29; 10000000=ADC30

ADC_IO_SEL4 (56H) ADC select enable register 4

Bit number	7	6	5	4	3	2	1	0
Symbol	ADC_IO_SEL4 [7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	ADC_IO_SEL4 [7:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00000001=ADC31; 00000010=ADC32; 00000100=ADC33; 00001000=ADC34; 00010000=ADC35; 00100000=ADC36; 01000000=ADC37; 10000000=ADC38

ADC_IO_SEL5 (57H) ADC select enable register 5

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	ADC_IO_SEL5 [4:0]				
R/W	-	-	-	R/W				
Reset value	-	-	-	0				

Bit number	Bit symbol	Description
7~5	--	Reserved
4~0	ADC_IO_SEL5 [4:0]	Enable the ADC control function that disables analog input pins 1: Select ADC function; 0: Not select ADC function 00001=ADC39; 00010=ADC40; 00100=ADC41; 01000=ADC42; 10000=ADC43;

13.2.2. Module Switch Control Register

PD_ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	-	PD_LVDT	-	PD_XTAL_32K	-	PD_ADC
R/W	-	R/W	-	R/W	-	R/W
Reset value	-	1	-	1	-	1

Bit number	Bit symbol	Description
0	PD_ADC	Analog ADC shutdown control register 0: ADC module works normally; 1: ADC module does not work

13.2.3. ADC Configuration Register

ADC_CFG_SEL (32H) ADC configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	ADCWNUM					ADC_I_SEL	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6~2	ADCWNUM	Selection of distance conversion interval time after sampling: (3+ADCWNUM)*T_{ADCK}
1	ADC_I_SEL[1]	ADC select comparator bias current, 1: 4 μA; 0: 5 μA
0	ADC_I_SEL[0]	ADC select buffer bias current, 1: 4 μA; 0: 5 μA

13.2.4. ADC Comparator Offset Cancellation Selection Register

ADC_CFG_SEL1 (42H) ADC comparator offset cancellation selection register

Bit number	7	6	5	4
Symbol	-	-	ADC_VREF_SEL	ADC_VREF_VOL_SEL
R/W	-	-	R/W	R/W
Reset value	-	-	0	0
Bit number	3	2	1	0
Symbol	VREF_IN_ADC_SEL		CTRL_SEL	

R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	0

Bit number	Bit symbol	Description
5	ADC_VREF_SEL	ADC reference voltage selection: 0: Select VCC as the output signal; 1: Select the voltage output by the ADC_VREF module as the reference voltage.
4	ADC_VREF_VOL_SEL	ADC_VREF output mode selection: 0: 2V as ADC reference voltage; 1: 4V as ADC reference voltage. When ADC_VREF output mode is 2V/4V, it is recommended to select 3MHz for ADC frequency division clock
3~2	VREF_IN_ADC_SEL	Voltage selection input to the internal ADC channel of the chip 00: 1.362V; 01: 2.253V; 10: 3.111V; 11: 4.082V;
1~0	CTRL_SEL	ADC offset elimination timing selection, the default value is 10: 00/01: first offset elimination and then sampling; 10/11: offset elimination and sampling are performed at the same time, 10 first-stage comparator switches are turned off at the end; 11: all switches are turned off at the same time

13.3. ADC Important Point

Timing requirements: (3+ADCWNUM) *TADCK >4*TADCK
ADCK: ADC clock 8 MHz/6 MHz/4 MHz/3MHz;
ADCCKV: ADC comparator offset cancellation analog input clock 12 MHz/8 MHz/4 MHz/2 MHz;
Voltage settling time after ADC input signal plus RC filter>= 2*(ADC conversion time);
ADC conversion time:

formula	Description
t_{ADC} =t_1+t_2+t_3+200ns	ADC detection time
t_1 = 4*(ADC_SPT+1) *T_{ADCK}	ADC sampling time
t_2=(ADCWNUM+3+SAMDEL)*T_{ADCK}	Distance conversion interval time after sampling
t_3=(2*1+12)*T_{ADCK}	Sampling delay time

1. ADC_SPT: ADC sampling time configuration register (ADC_SPT=0~255).
   SAMDEL: Sampling delay time selection (SAMDEL=0: 0; 1: 2; 2: 4; 3: 8).
2. **When selecting VCC as the ADC reference voltage,** when the power supply voltage fluctuates greatly or drops, the VCC voltage value can be inversely calculated by the formula ADCINNER_Data/ VREF_IN_ADC_SEL = 4096/VCC, and the Vin voltage value can be inversely calculated by the formula Vin_Data/Vin=4096/VCC.
   ADCINNER_Data: ADC internal channel data;
   Vin_Data： ADC input channel data;
   Vin： Input voltage;
   VREF_IN_ADC_SEL: Need to read the chip calibration value,
   Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL, VREF_IN_ADC_SEL needs to read the chip calibration value, first obtain the internal channel data, and then obtain the input voltage Vin_Data data, and the interval between two data acquisitions should be as short as possible;
   When ADC_VREF_VOL _SEL 2V/4V reference voltage is selected, It is recommended to select 3MHz for ADC frequency division clock, The voltage value of Vin can be inversely calculated by the formula Vin_Data/Vin=4096/ADC_VREF_VOL _SEL.
   Vin_Data: ADC input channel data;
   Vin: Input voltage (0~ADC_VREF_VOL _SEL);
   VREF_IN_ADC_SEL: Need to read the chip calibration value,
   Vin = (Vin_Data/ADCINNER_Data)*VREF_IN_ADC_SEL, ADC_VREF_VOL _SEL needs to read the chip calibration value, Get the internal channel data first, then get the input voltage Vin_Data data, The interval between two data acquisitions should be as short as possible;
3. ADC input interrupt conditions： The configuration sequence is ADC_IO_SEL enable->ADC interrupt enable->ADC_ADDR(Address and ADC_IO_SEL must correspond)-> ADC_START, Note on initial configuration timing during application. If there is an application where ADC and IO port functions are multiplexed, you need to pay attention to the switching timing, If ADC_IO_SEL is enabled or disabled or Address does not correspond to ADC_IO_SEL, ADC scanning cannot be turned on, and the configuration sequence must be

followed： ADC_IO_SEL enable->ADC interrupt enable->ADC_ADDR(Address and ADC_IO_SEL must correspond）-> ADC_START, to enable ADC scan

4. {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41CA] ADC internal channel input voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41CB] ADC internal channel input voltage calibration value low eight bits,
   Read the 1.362V calibration value of the chip's information address ADC internal channel input voltage;

   {SPROG_ADDR_H, SPROG_ADDR_L} = [0x41CC] ADC internal channel input voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41CD] ADC internal channel input voltage calibration value low eight bits,
   Read the chip information address ADC internal channel input voltage 2.253V calibration value;

   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41CE] ADC internal channel input voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41CF] ADC internal channel input voltage calibration value low eight bits,
   Read the chip information address ADC internal channel input voltage 3.111V calibration value;

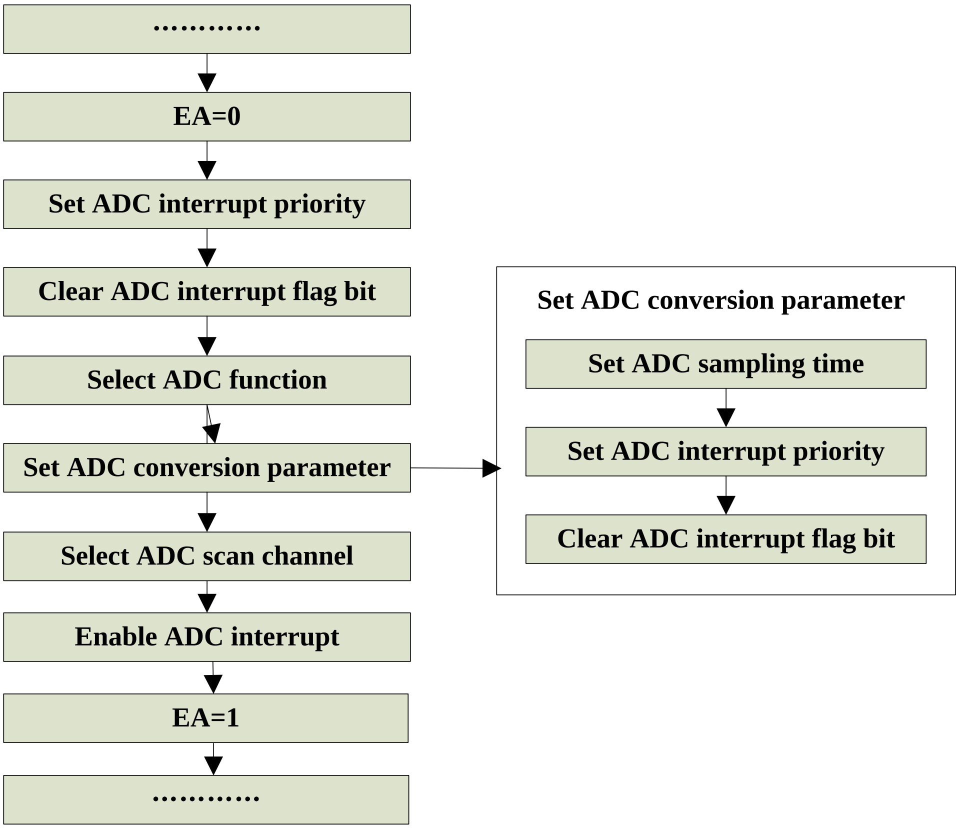
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D0] ADC internal channel input voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D1] ADC internal channel input voltage calibration value low eight bits,
   Read the chip information address ADC internal channel input voltage 4.082V calibration value;

   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D2] ADC_VREF 2V voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D3] ADC_VREF 2V voltage calibration value low eight bits,
   Read the calibration value of the chip information address ADC_Vref2V;

   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D4] ADC_VREF 4V voltage calibration value high eight bits,
   {SPROG_ADDR_H, SPROG_ADDR_L}= [0x41D5] ADC_VREF4V voltage calibration value low eight bits,
   Refer to Chapter 3 to read Flash information steps.

5. When the pin is configured as ADC function, the pin needs to be configured as IO input mode, and other multiplexing functions are turned off, such as pull-up resistors, etc.

13.4. ADC Configuration Process



ADC configuration flow chart

14. LVDT

The BF7515CM44-LJTX series supports low voltage alarm function, which can effectively monitor the dynamic changes of voltage. Support 8 voltage levels, respectively: 2.7V/3.0V/3.3V/3.6V/3.8V/4.0V/4.2V/4.4V (preset point step-down interrupt, hysteresis 0.1V generates corresponding step-up interrupt). When the voltage monitoring is configured with the above threshold, the voltage drop to this threshold will trigger a low-voltage interrupt, and the system can handle the low-voltage interrupt appropriately according to application needs.

14.1. LVDT Related Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xD5	INT_POBO_STAT	RW	xxxx_xx00b	LVDT Boost/Buck interrupt status register
0xE1	IRCON2	RW	0000_0000b	Interrupt flag register 2
0xE7	IEN2	RW	0000_0000b	Interrupt enable register 2
0xF4	IPL2	RW	0000_0000b	Interrupt priority register2

LVDT SFR register list

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x2C	SEL_LVDT_VTH	RW	xxxx_x000b	LVDT threshold selection register
0x2D	PD_ANA	RW	x111_xx11b	Analog module switch register
0x65	SEL_LVDT_DELAY	RW	xxxx_xx00b	LVDT delay control register

LVDT secondary bus register list

14.1.1. LVDT Boost/Buck Interrupt Status Register

INT_POBO_STAT (D5H) LVDT Boost/buck interrupt status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INT_PO_STAT	INT_BO_STAT
R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

Bit number	Bit symbol	Description
1	INT_PO_STAT	LVDT boost interrupt status. 1: Boost interrupt is valid; 0: Boost interrupt is invalid.
0	INT_BO_STAT	LVDT buck interrupt status. 1: The buck interrupt is valid; 0: The buck interrupt is invalid

14.1.2. Interrupt Flag Register 2

IRCON2 (E1H) Interrupt flag register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
0	IE8	LVDT interrupt flag 1: With LVDT interrupt flag 0: Clear LVDT interrupt flag

14.1.3. Interrupt Enable Register 2

IEN2 (E7H) Interrupt enable register 2

Bit number	7	6	5	4	3	2	1	0
Symbol	EX15	EX14	EX13	EX12	EX11	EX10	EX9	EX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
0	EX8	LVDT interrupt enable 1: LVDT interrupt enable; 0: LVDT interrupt disable

14.1.4. Interrupt Priority Register2

IPL2 (F4H) Interrupt priority register2

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL2.7	IPL2.6	IPL2.5	IPL2.4	IPL2.3	IPL2.2	IPL2.1	IPL2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
0	IPL2.0	LVDT priority selection bit. 1: LVDT interrupt is high priority; 0: LVDT interrupt is low priority

14.2. LVDT Secondary Bus Register

14.2.1. LVDT Threshold Selection Register

SEL_LVDT_VTH (2CH) LVDT threshold selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	SEL_LVDT_VTH		
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	SEL_LVDT_VTH	LVDT threshold selection, the corresponding threshold is shown in the table "Threshold and Delay Selection" 000=2.7V; 001=3.0V; 010=3.8V; 011=4.2V; 100=3.3V; 101=3.6V; 110=4.0V; 111=4.4V

14.2.2. Module Switch Control Register

PD_ANA (2DH) Module switch control register

Bit number	7	6	5	4	3~1	0
Symbol	-	PD_LVDT	-	PD_XTAL_32K	-	PD_ADC
R/W	-	R/W	-	R/W	-	R/W
Reset value	-	1	-	1	-	1

Bit number	Bit symbol	Description
6	PD_LVDT	LVDT control register 1: Closed 0: Open, closed by default

14.2.3. LVDT Delay Control Register

SEL_LVDT_DELAY (65H) LVDT delay control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

R/W	-	-	-	-	-	-	R/W	R/W
Reset value	-	-	-	-	-	-	0	0

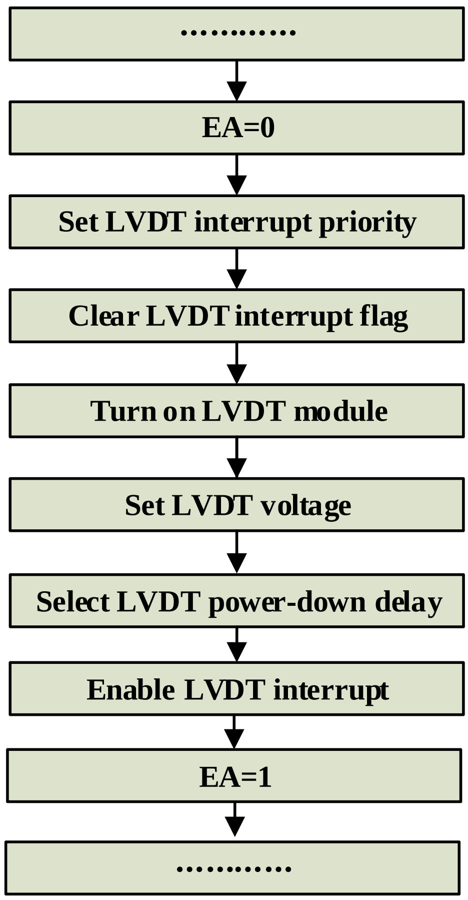
Bit number	Bit symbol	Description
1~0	SEL_LVDT_DELAY	Select signal, select LVDT power-down delay; 00: Delay time 1; 01: Delay time 2; 10: Delay time 3; 11: Delay time 4

SEL_LVDT_VTH	SEL_LVDT_DELAY	LVDT			
		Power down threshold (V)	Recovery threshold (V)	Hysteresis (mV)	Delay (µs)
000	00	2.7	2.8	124	7.9
	01	2.7	2.8	125	14.9
	10	2.7	2.8	125	29.1
	11	2.7	2.8	127	57.3
001	00	3.0	3.1	117	8.7
	01	3.0	3.1	117	16.5
	10	3.0	3.1	118	32.3
	11	3.0	3.1	120	63.8
010	00	3.8	3.9	123	10.2
	01	3.8	3.9	123	19.6
	10	3.8	3.9	124	38.5
	11	3.8	3.9	126	76.3
011	00	4.2	4.3	124	10.8
	01	4.2	4.3	125	20.7
	10	4.2	4.3	126	40.8
	11	4.2	4.3	128	80.8
100	00	3.3	3.4	93	9.3
	01	3.3	3.4	94	17.7
	10	3.3	3.4	94	34.8
	11	3.3	3.4	95	68.7
101	00	3.6	3.7	109	9.8
	01	3.6	3.7	110	18.8
	10	3.6	3.7	111	37
	11	3.6	3.7	113	73.2
110	00	4.0	4.1	135	10.5
	01	4.0	4.1	136	20.1
	10	4.0	4.1	137	39.7
	11	4.0	4.1	139	78.6

111	00	4.4	4.5	83	11.1
	01	4.4	4.5	83	21.3
	10	4.4	4.5	84	41.9
	11	4.4	4.5	68	82.8

Threshold and delay selection

14.3. LVDT configuration process



LVDT configuration flow chart

15. LED/LCD

The module can be configured with three drive modes: LED matrix drive mode, LED dot matrix drive mode, LCD drive mode. Through register configuration, only one mode of operation is supported at the same time.

All of the above driving methods, the total IO port switch is configurable, the scanning mode is configurable, the software controls the LED scanning to start, the interrupt mode scanning once interrupts and stops, and the cycle mode automatically starts the next frame scanning after one frame is scanned, without interruption If you want to stop, you need to turn off the scan enable by the software. When the scan enable is turned off, all states of the module are reset. Including LED controller and LCD controller.

15.1. LED Dot Matrix Driver

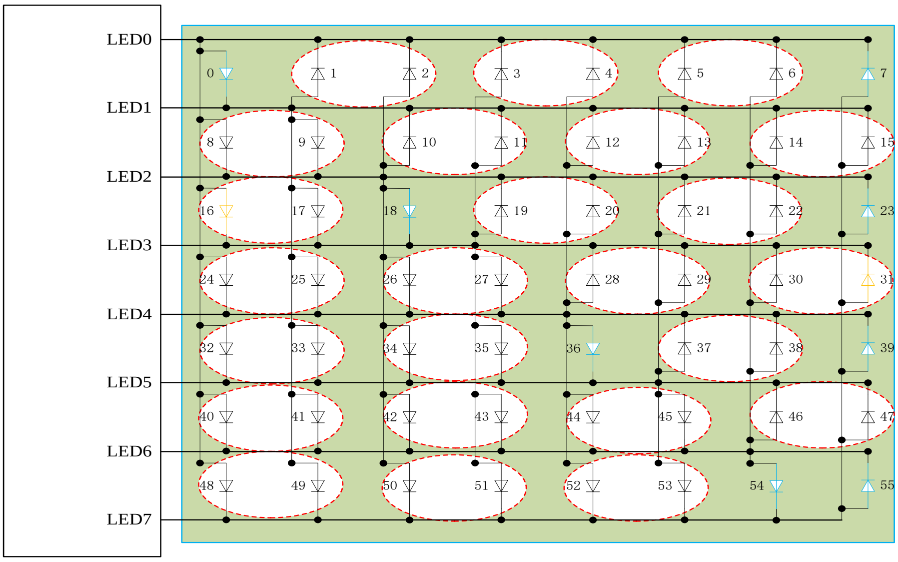
Features of LED dot matrix drive mode:

- Supports up to 56 lights LED drive, configurable to choose matrix 4*5, 5*6, 6*7, 7*8, of which matrix 4*5 supports two IO enable;
- Dual lamps are turned on at the same time, the specific distribution is shown in the dot matrix description below;
- Single lamp on-time setting file: 8-bit register, configurable range is 16μs-4.096ms, step is 16μs;
- Each lamp driving time is individually selectable;
- IO ports have multiple multiplexing relationships. Each IO port needs to be configured through software to switch to LED port. According to the LED dot matrix mode selection, the LED function of LED0~LED7 corresponding to IO port will be automatically turned on. The starting port LED0 supports the selection of PB0~PB7. Other mouth sequence circulation;
- 56 light dot matrix Address is unique, see the dot matrix description below, used to input switch light information;

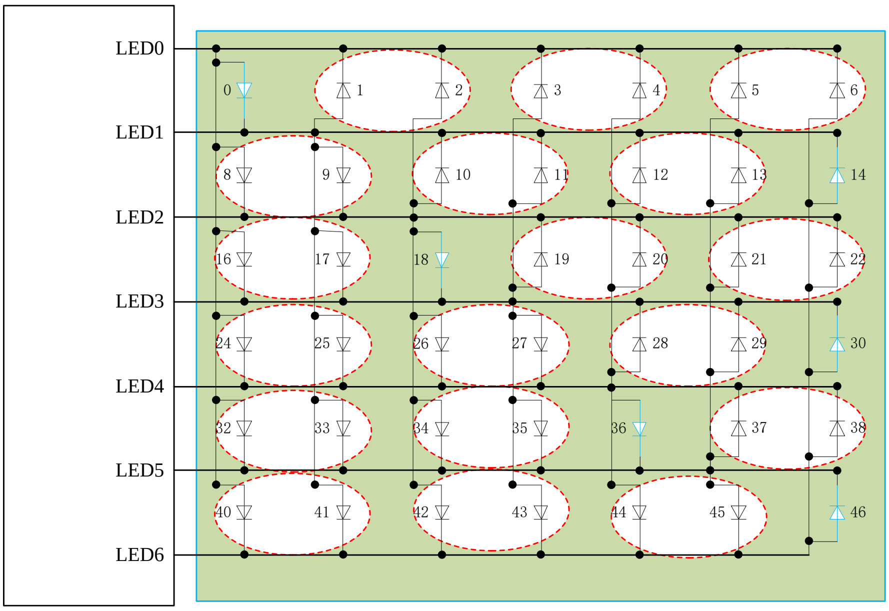
15.1.1. LED Dot Matrix Description

16. The LED dot matrix is a universal 7*8 dot matrix, and uses the dual lamp mode, that is, two lamps are lit at a time (common cathode). Corresponding to LED0~LED7 ports, up to 7x8=56 lamps can be configured to drive. The lamp address of the corresponding position is marked in the 7*8 dot matrix in the figure below. The display configuration in the SRAM corresponds to the lighting condition of the corresponding address (1 means lighting, 0 means no light), the hardware code needs to analyze the light address and the current scan address to automatically complete the corresponding IO port output control. Configurable dot matrix 4*5, 5*6, 6*7, 7*8, different size dot matrix, the corresponding lamp address remains unchanged.

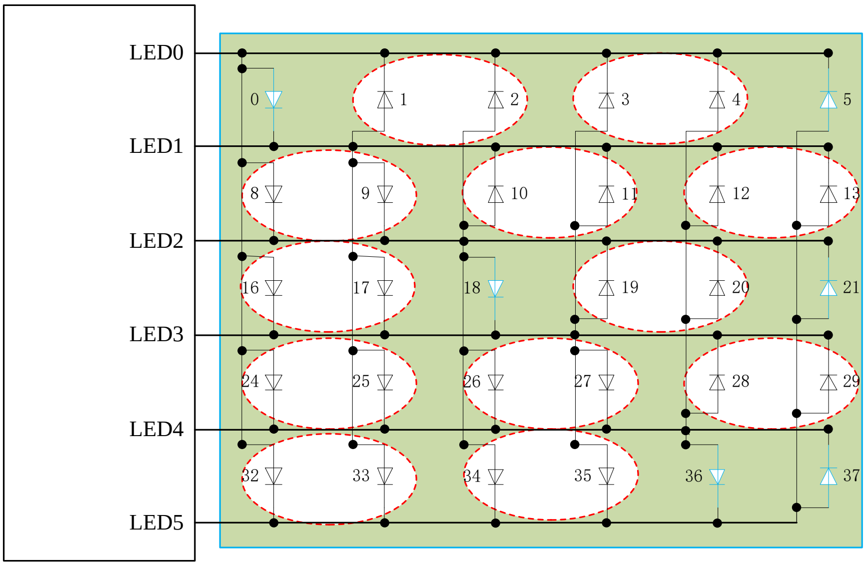
7*8 dot matrix:



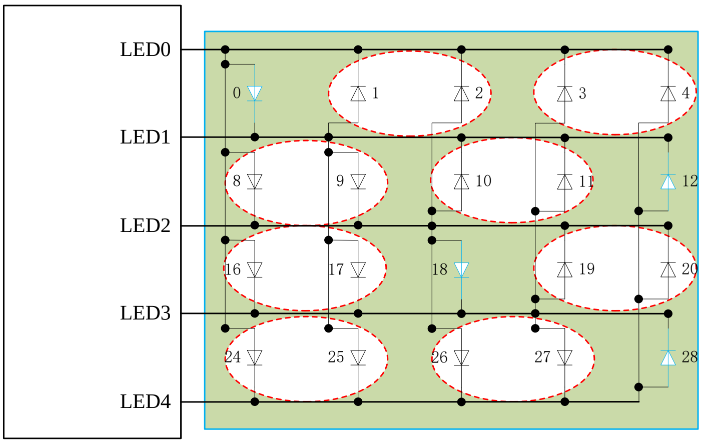
6*7 dot matrix:



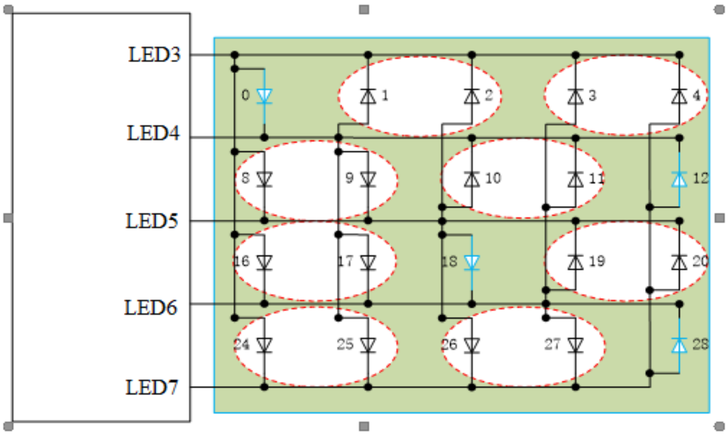
5*6 dot matrix:



4*5 dot matrix: Take LED0 as the starting port:

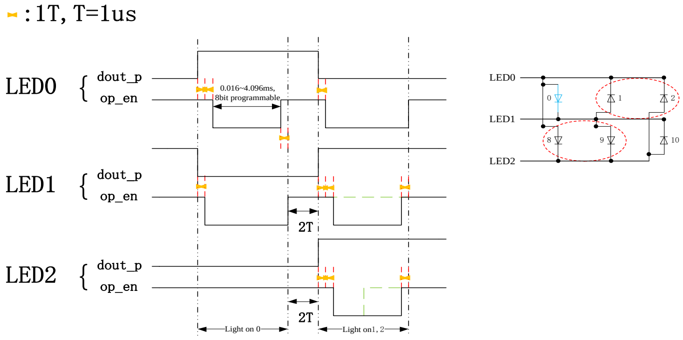


4*5 dot matrix: Take LED3 as the starting port:



Dot matrix scan timing example:

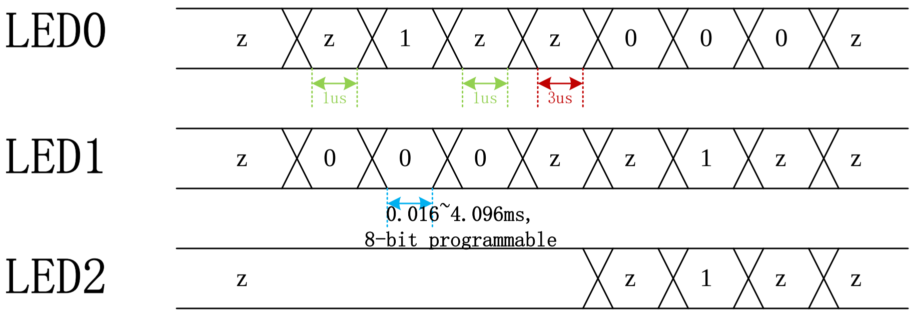
Take lighting 0, 1, 2 as an example, the detailed digital output interface control sequence is shown in the figure below:



Note:

1. dout_p: output data signal, 2. op_en: output enable signal

Combined with the above figure, the schematic diagram of the IO port status is as follows:



LED scanning timing diagram

The starting port LED0 of the series can choose the specific position of the PAD, and DUTY_SEL[2] = 0.

LED_IO_START	dot matrix	order
000：PB0	7*8	PB0→PB1→PB2→PB3→PB4→PB5→PB6→PB7
	6*7	PB0→PB1→PB2→PB3→PB4→PB5→PB6
	5*6	PB0→PB1→PB2→PB3→PB4→PB5
	4*5	PB0→PB1→PB2→PB3→PB4
001：PB1	7*8	PB1→PB2→PB3→PB4→PB5→PB6→PB7→PB0
	6*7	PB1→PB2→PB3→PB4→PB5→PB6→PB7
	5*6	PB1→PB2→PB3→PB4→PB5→PB6
	4*5	PB1→PB2→PB3→PB4→PB5
010：PB2	7*8	PB2→PB3→PB4→PB5→PB6→PB7→PB0→PB1
	6*7	PB2→PB3→PB4→PB5→PB6→PB7→PB0
	5*6	PB2→PB3→PB4→PB5→PB6→PB7
	4*5	PB2→PB3→PB4→PB5→PB6
……	……	and so on

LED dot matrix drive LEDX arrangement order

15.1.2. Display Configuration Address

LED dot matrix drive mode corresponding to display configuration:
DX indicates whether the light is selected or not, 0: not bright, 1: bright;
Dx_SEL indicates that the light is selected for the lighting cycle, 0: select the first segment of the light cycle, 1: select the second segment of the light cycle.

Address	7	6	5	4	3	2	1	0
1000H	D7	D6	D5	D4	D3	D2	D1	D0
1001H	D15	D14	D13	D12	D11	D10	D9	D8
1002H	D23	D22	D21	D20	D19	D18	D17	D16
1003H	D31	D30	D29	D28	D27	D26	D25	D24
1004H	D39	D38	D37	D36	D35	D34	D33	D32
1005H	D47	D46	D45	D44	D43	D42	D41	D40
1006H	D55	D54	D53	D52	D51	D50	D49	D48
1007H	D7_SEL	D6_SEL	D5_SEL	D4_SEL	D3_SEL	D2_SEL	D1_SEL	D0_SEL
1008H	D15_SEL	D14_SEL	D13_SEL	D12_SEL	D11_SEL	D10_SEL	D9_SEL	D8_SEL
1009H	D23_SEL	D22_SEL	D21_SEL	D20_SEL	D19_SEL	D18_SEL	D17_SEL	D16_SEL
100AH	D31_SEL	D30_SEL	D29_SEL	D28_SEL	D27_SEL	D26_SEL	D25_SEL	D24_SEL
100BH	D39_SEL	D38_SEL	D37_SEL	D36_SEL	D35_SEL	D34_SEL	D33_SEL	D32_SEL
100CH	D47_SEL	D46_SEL	D45_SEL	D44_SEL	D43_SEL	D42_SEL	D41_SEL	D40_SEL
100DH	D55_SEL	D54_SEL	D53_SEL	D52_SEL	D51_SEL	D50_SEL	D49_SEL	D48_SEL

LED dot matrix drive mode corresponding display configuration table

15.1.3. LED Dot Matrix Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan on register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000b	LED cycle configuration register
0xB4	LED2_WIDTH	RW	0000_0000b	LED dot matrix drive mode cycle configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x31	LED_DRIVE	RW	xxxx_0000b	LED port drive capability configuration register
0x58	LED_IO_START	RW	xxxx_x000b	LED scan start selection register

15.1.3.1. LED Scan on Register

SCAN_START (AFH) LCD, LED scan on register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LCD, LED scan on register 1: Scan on; 0: Scan off

15.1.3.2. LED Control Register

DP_CON (B1H) LCD, LED control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	IO_ON	DUTY_SEL			DPSEL	SCAN_MODE	COM_MOD

R/W	-	R/W	R/W			R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LED dot matrix drive mode dot matrix selection configuration register Bit[1:0]: 00: 4x5 lattice; 01: 5x6 lattice; 10: 6x7 lattice; 11: 7x8 lattice Bit [2]: 0: Take LED0 as the starting port 1: 4x5 dot matrix-LED3 (as the starting port to enable)
2	DPSEL	LCD, LED select control bit 0: Select LCD driver, LED driver is invalid 1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration 1: Cyclic scan mode; 0: Interrupt scan mode
0	COM_MOD	High-current IO port driver enable 1: COM port function is locked and works as a high-current IO port; 0: COM port function is not locked and can be configured as other functions; When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED/LCD scan configuration is invalid

15.1.3.3. LED Mode Register

DP_MODE (B2H) LCD, LED mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_CKSEL		LCD_RSEL	LCD_FCSEL		LCD_RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	LED_MOD	LED drive mode selection register

		1: Serial dot matrix scanning 0: Row and column matrix scan

15.1.3.4. LED Period Configuration Register

SCAN_WIDTH (B3H) LED period configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the first segment of the lamp cycle configuration: period=(scan_width+1)*16us, the support configuration range is 0.016~4.096ms; When on-time 1<on-time 2, the scan time of this group is on-time 2.

LED2_WIDTH (B4H) LED dot matrix drive mode cycle configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED dot matrix drive mode, the corresponding single lamp lighting time configuration register-the second stage of lamp cycle configuration Period = (led2_width+1)*16us Note: This register is only applicable to LED dot matrix drive mode: when the on time 1 is greater than the on time 2, the scan time of this group is on time 1.

15.1.3.5. LED Interrupt Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
0	INT_LED_STAT	LED interrupt status flag, write 0 to clear this bit, write SCAN_START operation can also be cleared 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	EX6	LED/LCD interrupt enable 1: LED/LCD interrupt enable; 0: LED/LCD interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IE6	LED/LCD interrupt flag 1: With LED/LCD interrupt flag 0: Clear LED/LCD interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IPL1.6	LED/LCD interrupt priority bit 1: LED/LCD interrupt is high priority; 0: LED/LCD interrupt is low priority

15.1.4. Secondary Bus Register

15.1.4.1. LED Port Drive Capability Configuration Register

LED_DRIVE (31H) LED port drive capability configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-			
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	For details, please refer to LED serial dot matrix drive current description

15.1.4.2. LED Scan Start Selection Register

LED_IO_START(58H) LED scan start selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset value	-	-	-	-	-	0	0	0

Bit number	Bit symbol	Description
2~0	--	LED port serial dot matrix start PAD selection (only for LED serial dot matrix scan, and DUTY_SEL[2] needs to be configured to 0) 000: PB0 port; 001: PB1 port; 010: PB2 port; 011: PB3 port; 100: PB4 port; 101: PB5 port; 110: PB6 port; 111: PB7 port; See the table "LED dot matrix drive LEDX arrangement order"

15.1.5. LED Serial Dot Matrix Drive Current Description

(Ta = 27°C, VCC = 5V, LED lamp voltage drop 1.8V~2.3V)

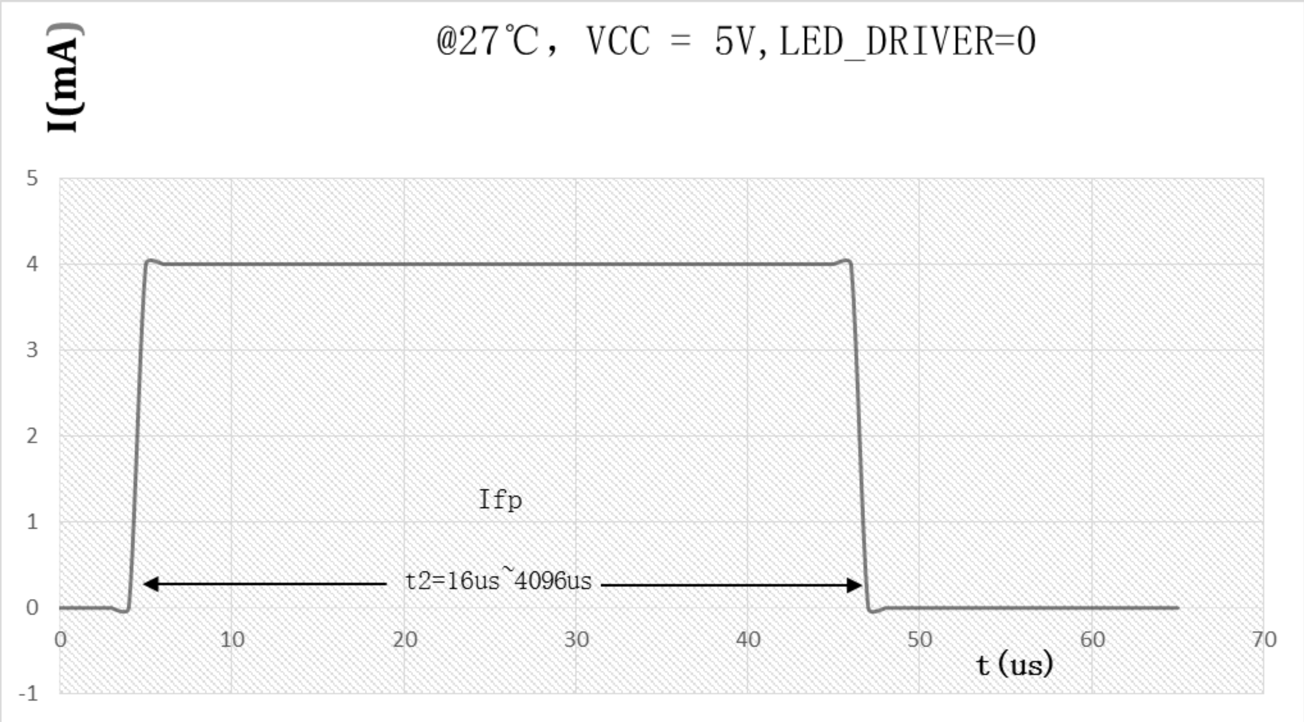
LED_DRIVE	Ifp(mA)
0	4
1	10
2	16
3	20
4	26
5	31
6	36
7	41
8	46
9	51
10	55
11	60
12	65
13	69
14	74
15	78

LED secondary bus drive current configuration register reference list

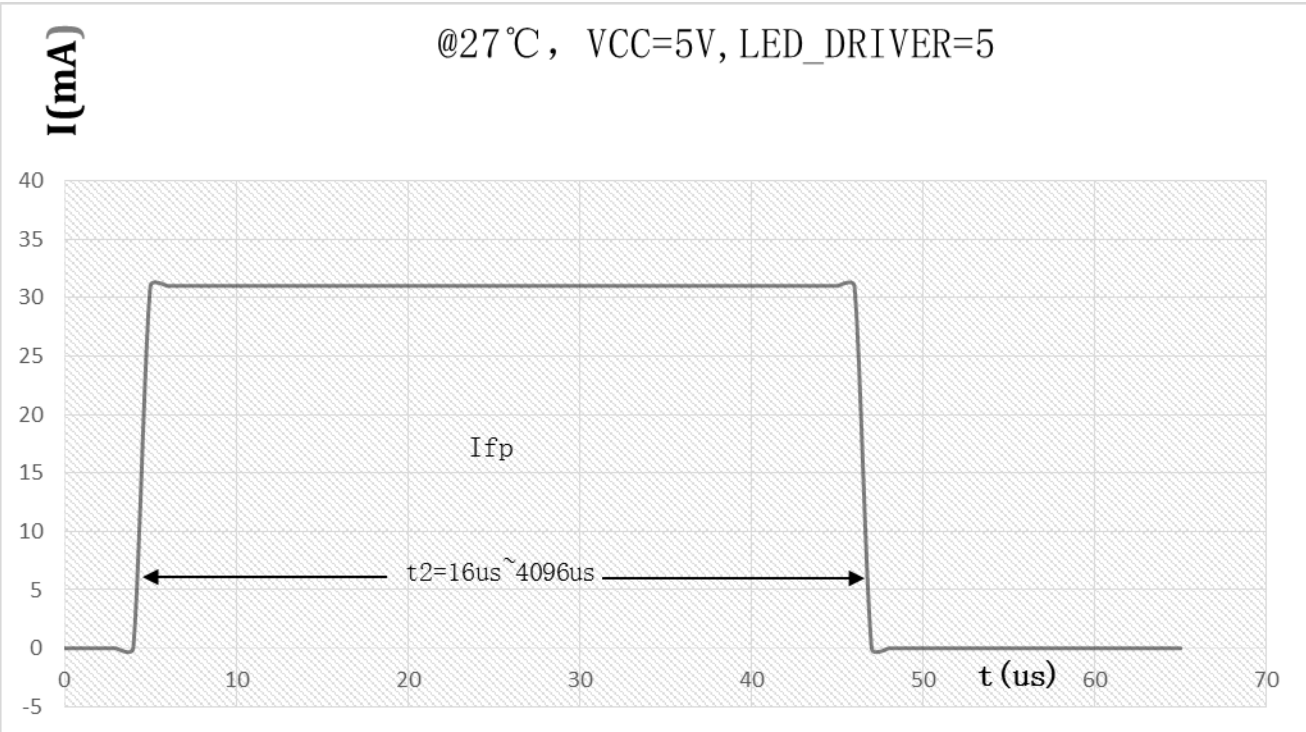
Note:

1. **LED drive current deviation range (±8%)@VCC=5V,Ta=(-40°C~105°C), the setting of LED_DRIVE is recommended to be less than the nominal Ifp current of the LED lamp, and the LED lamp to be driven should be forward LED lights with the same voltage VF.**
2. **LED_DRIVE:LED drive capability configuration register**
3. **Ifp: LED light conducts steady-state current.**

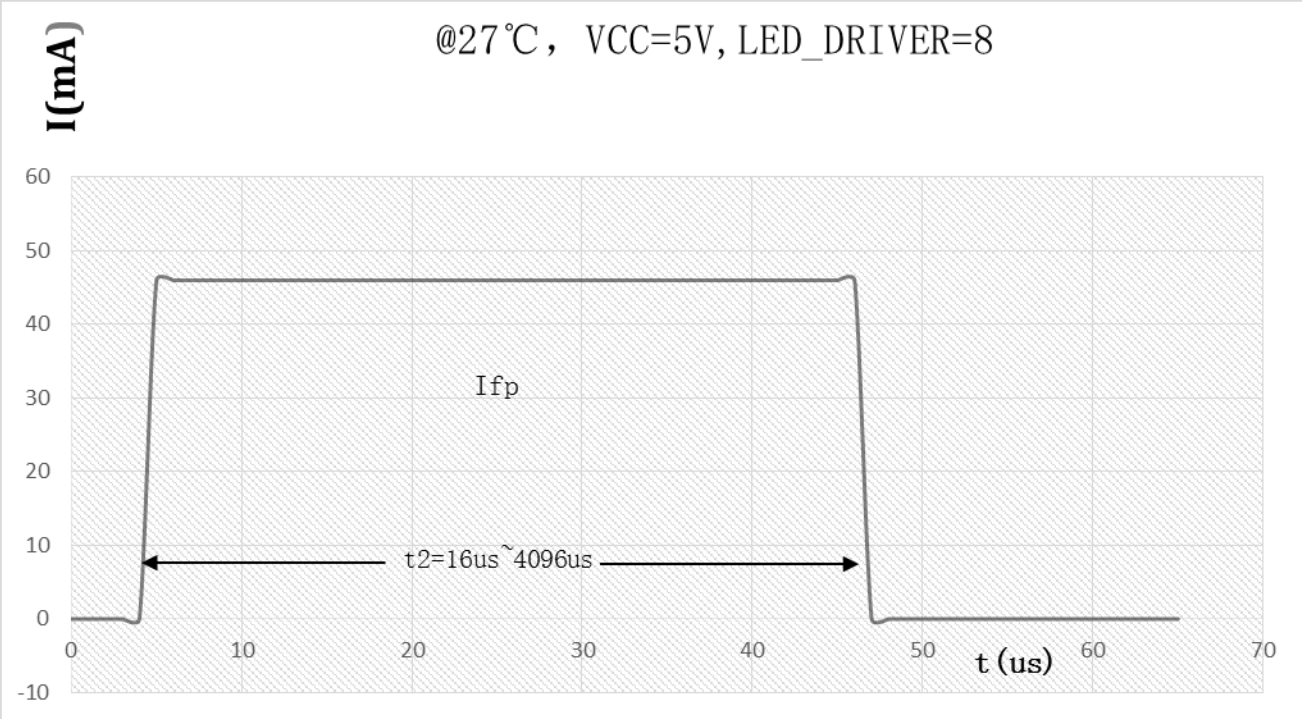
LED serial dot matrix drive current-time diagram under several common configurations:



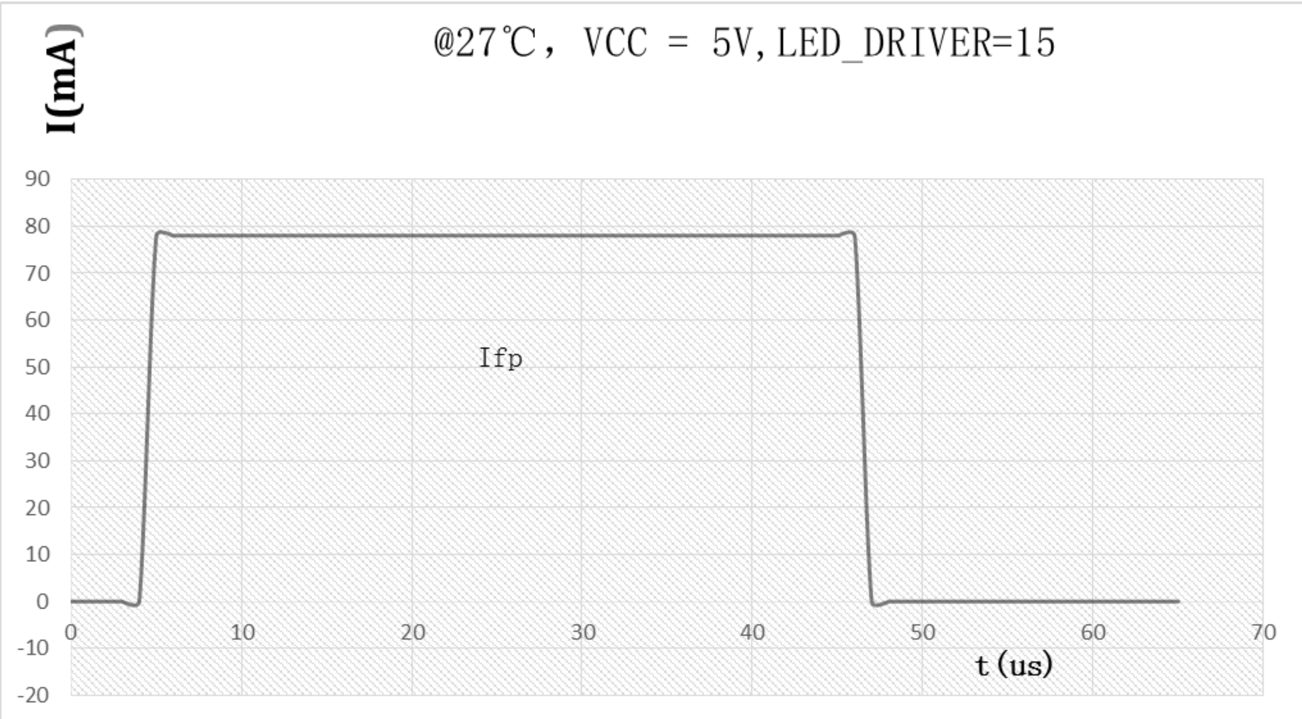
LED_DRIVER VS Time Figure1



LED_DRIVER VS Time Figure2

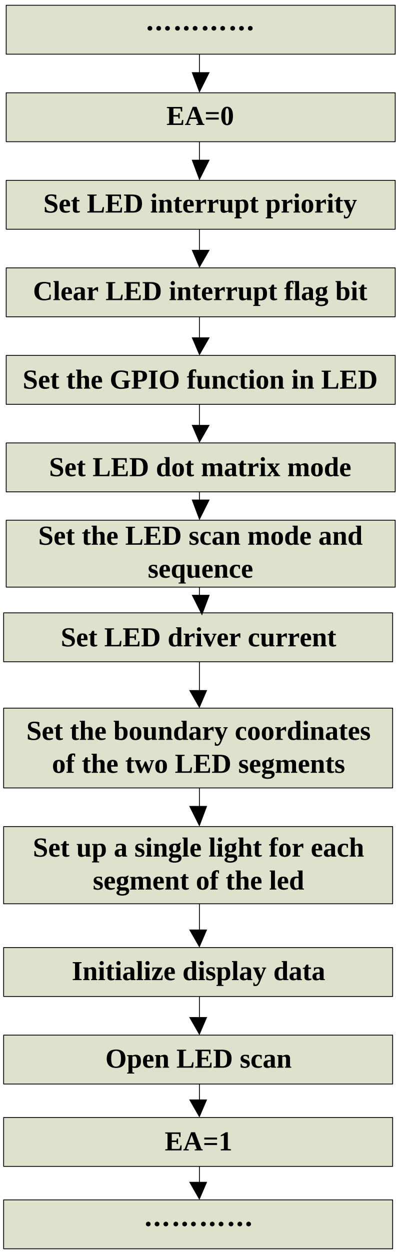


LED_DRIVER VS Time Figure3



LED_DRIVER VS Time Figure4

15.1.6. LED Dot Matrix Configuration Process



LED dot matrix configuration flow chart

15.2. LED Matrix Drive

Features of LED matrix drive mode:

- Support up to 8 COM x 8 SEG;
- The SEG and COM scan period share the same register SCAN_WIDTH, single SEG period= (scan_width+1) *16us, single COM period= (scan_width+1) *16us+8us;
- Single SEG conduction duty cycle: 1/8~8/8, configured by the register DP_CON[5:3];
- Support COM: 1 to 8, configured by the secondary bus register COM_IO_SEL;
- Support SEG: 1 to 8, configured by the secondary bus register SEG_IO_SEL configuration;
- Support LED row matrix 4*4 mode, COM/SEG port by the register COM_IO_SEL control, in this mode PB[0:3] for COM0-3 port, PB[4:7] for SEG0-3 port, support COM port forward and reverse configuration.

15.2.1. LED Matrix Driver Description

In LED matrix mode, SEGL port/COML port are optional, IO is freely configured, and configured by the following secondary bus addressing mode. The number of COML ports scanned is completely controlled by the COML port selection configuration register (COM_IO_SEL), and the duty cycle of the single COML port lighting interval is selectable from 1/8 to 8/8.

COM_IO_SEL (23H) COM port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

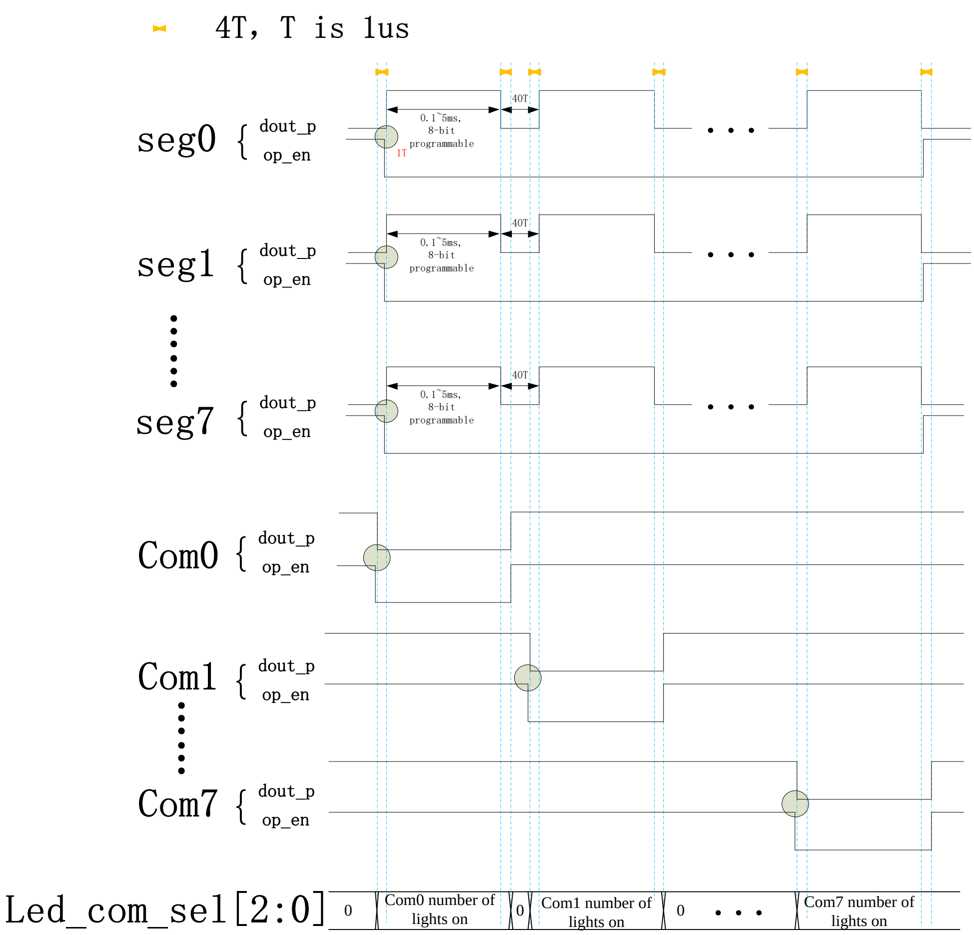
Bit number	Bit symbol	Description
7~0	--	COML port selection configuration register, the corresponding bit is 1 to select COML port function 1: Select COML port mode; 0: Select IO port mode Note: This register is valid when the LED matrix mode is selected, it is valid when the high current sink IO port drive is selected, and it is invalid in other cases

SEG_IO_SEL (24H) LED_SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEGL7	SEGL6	SEGL5	SEGL4	SEGL3	SEGL2	SEGL1	SEGL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LED_SEG0-7 port select configuration register, corresponding to bit 1, SEGLx is segment 1: select SEGMENT port mode; 0: select IO port mode

The SEG port output data corresponding to each COM port is stored in the SRAM to determine whether the light is on (1 means light, 0 means no light), the hardware code only needs to directly output data to the IO port according to the following sequence.



Timing diagram of LED matrix mode

15.2.2. Display Configuration Address

LED matrix drive mode corresponding display configuration:
SEGx means to choose whether to light up, 0: no light, 1: light

Address		7	6	5	4	3	2	1	0
1000H	COM0	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1001H	COM1	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1002H	COM2	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1003H	COM3	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1004H	COM4	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1005H	COM5	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1006H	COM6	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
1007H	COM7	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0

LED matrix drive mode corresponding display configuration table

15.2.3. LED Matrix Drive Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000b	LED cycle configuration register
0xB9	DP_CON1	RW	x000_0000b	LCD contrast Configuration Register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x23	COM_IO_SEL	RW	0000_0000b	COM selection configuration register
0x24	SEG_IO_SEL	RW	0000_0000b	LED_SEG0-7 port selection configuration register

15.2.3.1. LED Scan Open Register

SCAN_START (AFH) LCD, LED scan open regist

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LCD, LED scan on register 1: Scan on; 0: Scan off

15.2.3.2. LED Control Register

DP_CON (B1H) LCD, LED control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	IO_ON	DUTY_SEL			DPSEL	SCAN_MODE	COM_MOD
R/W	-	R/W	R/W			R/W	R/W	R/W
Reset value	-	0	0	0	0	0	O	0

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LED row and column drive mode single SEG port conduction duty cycle configuration register: 0: 1/8 duty cycle; 1: 2/8 duty cycle; 2: 3/8 duty cycle; 3: 4/8 duty cycle; 4: 5/8 duty cycle; 5: 6/8 duty cycle; 6: 7/8 duty cycle; 7: 8/8 duty cycle
2	DPSEL	LCD, LED selection control bit 0: Select LCD driver, LED driver is invalid 1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration 1: Cycle scan mode 0: Interrupt scan mode
0	COM_MOD	High current sink IO port drive enable 1: As a high current sink IO port; 0: Can be configured for other functions; When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED/LCD scan configuration is invalid

15.2.3.3. LED Mode Register

DP_MODE (B2H) LCD, LED mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_CKSEL		LCD_RSEL	LCD_FCSEL		LCD_RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7	LED_MOD	LED drive mode selection register 1: Serial dot matrix scan 0: Row and column matrix scan

15.2.3.4. LED Cycle Configuration Register

SCAN_WIDTH (B3H) LED cycle configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In the LED matrix drive mode, the corresponding single COM port scan time period = (scan_width+1)*16us, supports the configuration range 0.016~4.096ms

15.2.3.5. LED Row and Column Matrix 4*4 Mode Register

DP_CON1 (B9H) LCD contrast configuration register

Bit number	7	6	5	4
Symbol	-	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	VOL			
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
6	TRI_COM_INV	LED matrix 4*4 mode COM port reverse selection register in 4*4 mode, 1: Output high when COM is selected; 0: Output low when COM is selected
5	MATRIX_MOD	LED matrix 4*4 mode selection register 1: Select 4*4 mode, LED0~LED3 correspond, COM0~COM3 port selection, LED4~LED7 correspond, SEG0~SEG3 port selection; 0: Not select 4*4 mode

15.2.3.6. Interrupt Status Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
1	INT_LCD_STAT	LCD interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	EX6	LED/LCD interrupt enable 1: LED/LCD interrupt enable; 0: LED/LCD interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IE6	LED/LCD interrupt flag 1: LED/LCD interrupt flag 0: Clear LED/LCD interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-

R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IPL1.6	LED/LCD interrupt priority bit 1: LED/LCD interrupt is high priority; 0: LED/LCD interrupt is low priority

15.2.4. Secondary Bus Register

15.2.4.1. COM Port Selection Configuration Register

COM_IO_SEL (23H) COML select configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	COML7	COML6	COML5	COML4	COML3	COML2	COML1	COML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	In LED matrix drive mode, 4*4 mode is not selected: COM port select configuration register, the corresponding bit is 1, COMLx is common 1: Select the COM port function. 0: Select the I/O port mode In LED matrix drive mode, select 4*4 mode: COML0~ COML3 is common, and COML4~ COML7 is segment 1: Select COM port function or SEG port function; 0: Select the I/O port mode When the high current IO port drive is enabled: 1: Select the high-current I/O port 0: Select the I/O port mode

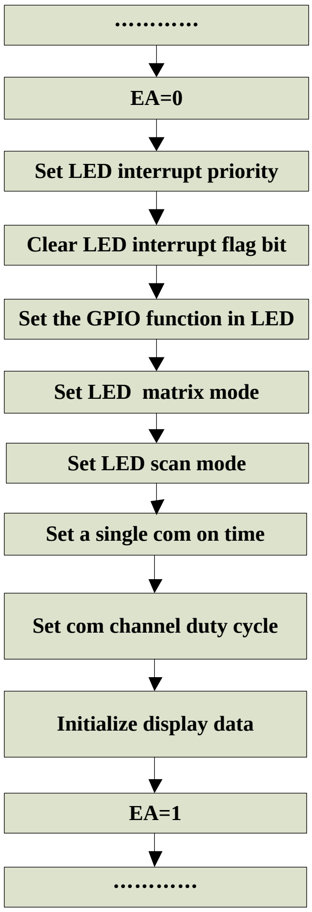
15.2.4.2. LED_SEG0-7 Port Selection Configuration Register

SEG_IO_SEL (24H) LED_SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEGL7	SEGL6	SEGL5	SEGL4	SEGL3	SEGL2	SEGL1	SEGL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LED_SEG0-7 port select configuration register, corresponding to bit 1, SEGLx is segment 1: select SEGMENT port mode; 0: select IO port mode

15.2.5. LED Matrix Configuration Process



LED matrix configuration flow chart

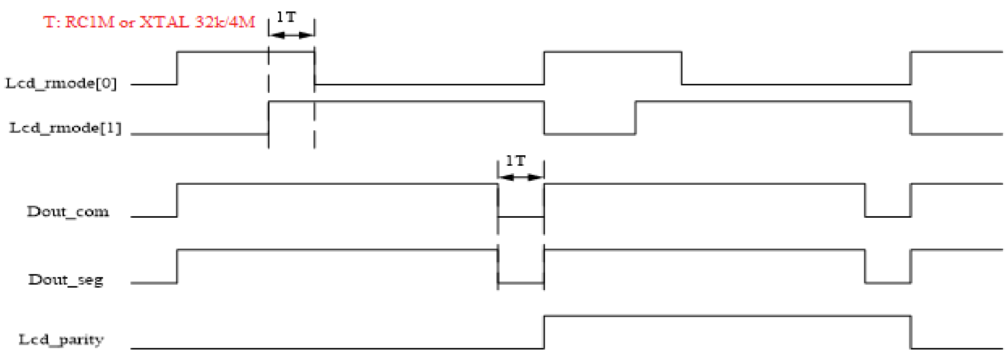
15.3. LCD Driver

Features of LCD drive mode:

- Supports duty cycles, selected according to register DUTY_SEL
  - 4 COM x 28 SEG (1/4 duty cycle, 1/3 bias)
  - 5 COM x 27 SEG (1/5 duty cycle, 1/3 bias)
  - 6 COM x 26 SEG (1/6 duty cycle, 1/3 or 1/4 bias)
  - 8 COM x 24 SEG (1/8 duty cycle, 1/4 bias)
- Support 2 drive modes: Traditional resistance mode (fast charging mode, slow charging mode), automatic switching mode between fast and slow charging.
- Support 3 kinds of bias resistance: 60k/225k/900k.
- Operating clocks: LIRC 32kHz, XTAL 32768Hz/4MHz, RC1MHz
  - Select RC1M, the lighting time of a single COM can be configured, the configuration range is 0.064~4.096ms, and the step is 64us;
  - Select LIRC 32KHz and XTAL 32768Hz, LCD conduction frequency is fixed at 64Hz (8COM configuration);
  - Select XTAL 4MHz, LCD conduction frequency is fixed at 7.8125kHz (8COM configuration)
- Support LCD contrast control, 0.531VDD~1.000VDD, 16-level contrast adjustment.
- The COM port is determined by the duty cycle configuration, and the SEG port is freely configured by the register.

15.3.1. LCD Driver Description

In LCD mode, the number of COM ports scanned is completely controlled by the drive mode duty cycle configuration register DUTY_SEL, and the SEG port selection is freely configured by LCD_IO_SEL_1, LCD_IO_SEL_2, LCD_IO_SEL_3, LCD_IO_SEL_4 registers, configured by the secondary bus addressing mode, LCD_IO_SEL_4 also determines the sharing, When the COM port in the mode is used as SEG port, whether the corresponding COM port is selected. SRAM stores the corresponding SEG port output data of each COM port to determine whether to light up (1 means light, 0 means no light). The hardware code needs to directly output data to the IO port control circuit according to the following sequence.



LCD timing diagram

DUTY_SEL	duty cycle&& bias	COM*SEG
000/110/111	1/4 duty cycle, 1/3 bias	4 COM x 16/24 SEG COM 0-3, SEG 0-23
001	1/8 duty cycle, 1/4 bias	8 COM x 16/24 SEG COM 0-7, SEG 0-23
010	1/4 duty cycle, 1/3 bias	4 COM x 20/28 SEG COM 0-3, SEG 0-23, COM 4-7 shared as SEG 24-27
011	1/5 duty cycle, 1/3 bias	5 COM x 19/27 SEG COM 0-4, SEG 0-23, COM 5-7 shared as SEG 25-27
100	1/6 duty cycle, 1/3bias	6 COM x 18/26 SEG COM 0-5, SEG 0-23, COM 6-7 shared as SEG 26-27
101	1/6 duty cycle, 1/4bias	6 COM x 18/26 SEG COM 0-5, SEG 0-23, COM 6-7 shared as SEG 26-27

LCD COM*SEG correspondence table

Analog IO implements the following truth table:

Bias voltage selection LCD_BIAS_SEL 0: 1/3 bias voltage 1: 1/4 bias voltage;

Odd and even frame selection LCD_PARITY 0: odd frame 1: even frame;

Resistance string selection LCD_RMODE 001: 20K 010: 75K 100: 300K;

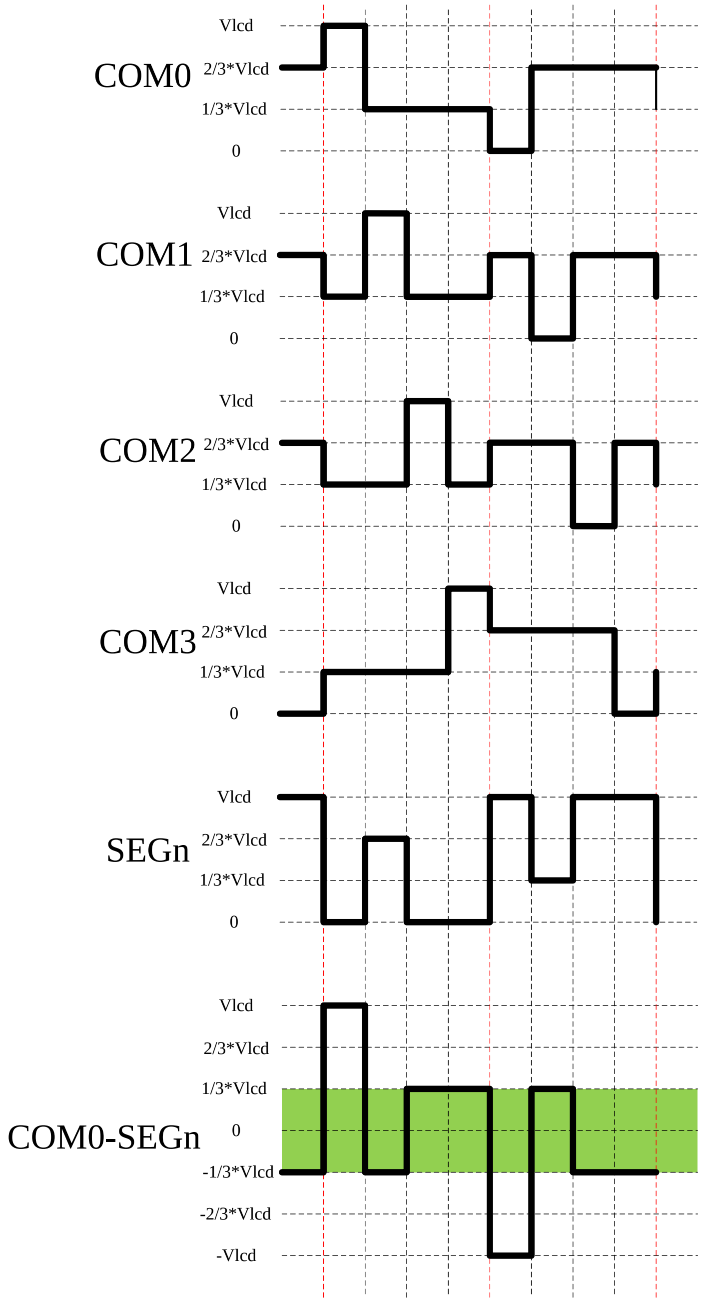
Data selection DOUT_PB (for example), compatible with the previous data line, the output function of the corresponding IO port is invalid (OP_EN_N=1);

COM truth table			
LCD_BIAS_SEL	LCD_PARITY	DOUT_PB	Output voltage value
0	0	0	1/3VLCD
0	0	1	VLCD
0	1	0	2/3VLCD
0	1	1	VSS
1	0	0	1/4VLCD
1	0	1	VLCD
1	1	0	3/4VLCD
1	1	1	VSS
SEG truth table			
LCD_BIAS_SEL	LCD_PARITY	DOUT_PB	Output voltage value
0	0	0	2/3VLCD
0	0	1	VSS
0	1	0	1/3VLCD
0	1	1	VLCD
1	0	0	2/4VLCD
1	0	1	VSS
1	1	0	2/4VLCD

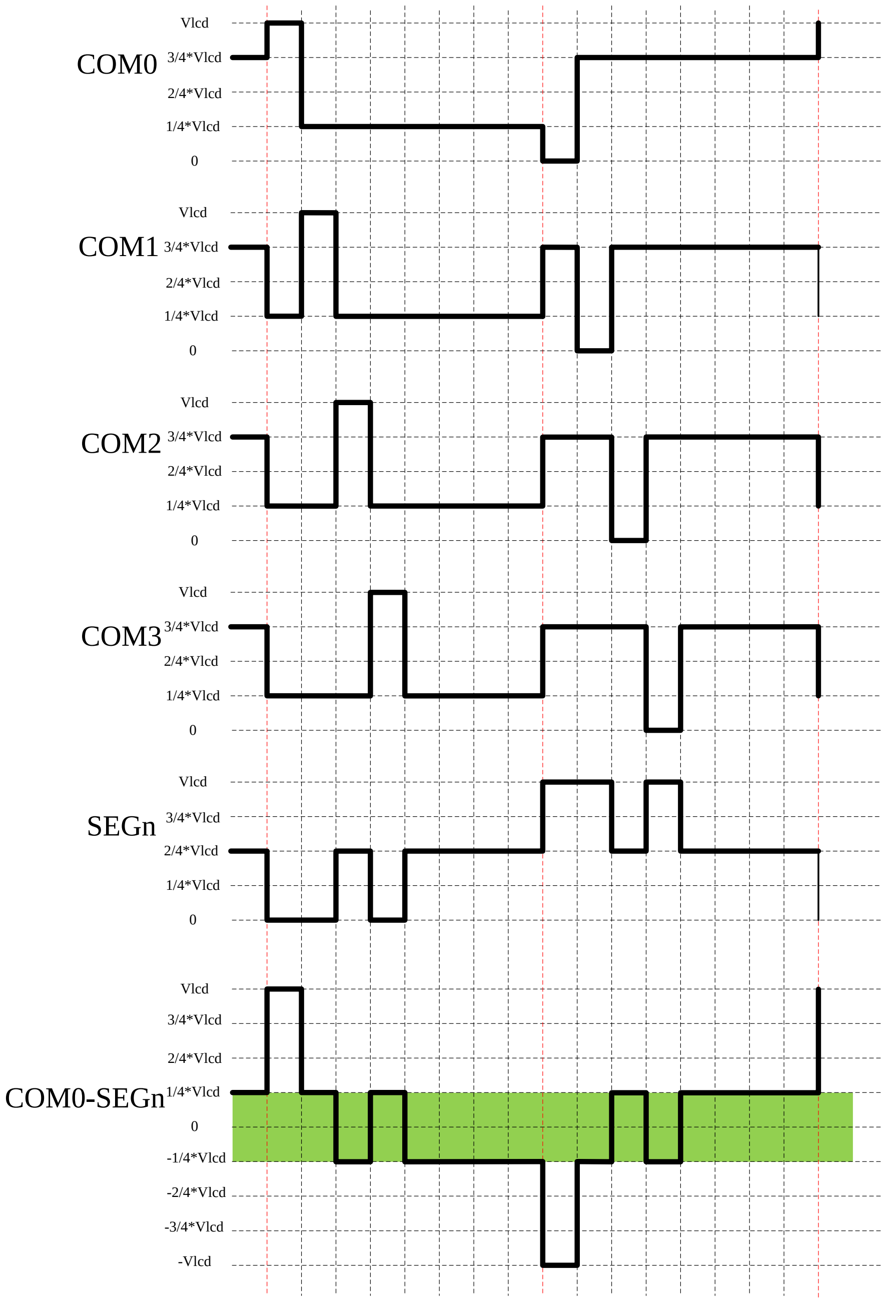
1	1	1	VLCD

LCD configure truth table

This realizes the bias voltage division sequence on the PAD, as shown in the figure below



LCD timing diagram (1/4 duty cycle, 1/3 bias)



LCD timing diagram (1/8 duty cycle, 1/4 bias)

15.3.2. Display Configuration Address

LCD drive mode corresponding display configuration:

SEGx means to choose whether to light up, 0: no light, 1: light;

Address	7	6	5	4	3	2	1	0
	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
1000H	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0
1001H	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1
1002H	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2
1003H	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
1004H	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
1005H	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
1006H	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
1007H	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
1008H	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
1009H	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
100AH	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
100BH	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
100CH	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
100DH	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
100EH	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
100FH	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
1010H	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
1011H	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
1012H	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
1013H	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19
1014H	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20
1015H	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21
1016H	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22
1017H	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23
1018H	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24
1019H			SEG25	SEG25	SEG25	SEG25	SEG25	SEG25
101AH			SEG26	SEG26	SEG26	SEG26	SEG26	SEG26
101BH					SEG27	SEG27	SEG27	SEG27

LCD drive mode corresponding display configuration table

15.3.3. LCD Register

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xAE	INT_PE_STAT	RW	0000_0000b	Interrupt status register
0xAF	SCAN_START	RW	xxxx_xxx0b	LCD, LED scan open register
0xB1	DP_CON	RW	x000_0000b	LCD, LED control register
0xB2	DP_MODE	RW	0000_0000b	LCD, LED mode register
0xB3	SCAN_WIDTH	RW	0000_0000b	LED cycle configuration register
0xB9	DP_CON1	RW	x000_0000b	LCD contrast configuration register
0xE6	IEN1	RW	0000_00xxb	Interrupt enable register 1
0xF1	IRCON1	RW	0000_00xxb	Interrupt flag register 1
0xF6	IPL1	RW	0000_00xxb	Interrupt priority register1

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x1F	LCD_IO_SEL_1	RW	0000_0000b	LCD_SEG0-7 port selection configuration register
0x20	LCD_IO_SEL_2	RW	0000_0000b	LCD_SEG8-15 port selection configuration register
0x21	LCD_IO_SEL_3	RW	0000_0000b	LCD_SEG16-23 port selection configuration register
0x22	LCD_IO_SEL_4	RW	xxxx_0000b	LCD_SEG24-27 port selection configuration register
0x63	XTAL_CLK_SEL	RW	xxxx_xxx0b	Crystal frequency selection register

15.3.3.1. LCD Scan Open Register

SCAN_START (AFH) LCD, LED scan open register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	LCD, LED scan on register 1: Scan on; 0: Scan off

15.3.3.2. LCD Control Register

DP_CON (B1H) LCD, LED control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	IO_ON	DUTY_SEL			DPSEL	SCAN_MODE	COM_MOD
R/W	-	R/W	R/W			R/W	R/W	R/W
Reset value	-	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6	IO_ON	LCD/LED scanning corresponds to the total control bit of all IO ports 0: Close IO; 1: Open IO
5~3	DUTY_SEL	LCD drive mode duty cycle configuration register 000: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG) COM port: COM0-3, SEG port: SEG0-23 001: 1/8 duty cycle, 1/4 bias (8 COM X 16/24SEG) COM port: COM0-7, SEG port: SEG0-23 010: 1/4 duty cycle, 1/3 bias (4 COM X 20/28 SEG) COM port: COM0-3, SEG port: SEG0-23, COM4-7 shared as SEG24-27 011: 1/5 duty cycle, 1/3 bias (5 COM X 19/27 SEG) COM port: COM0-4, SEG port: SEG0-23, COM5-7 shared as SEG25-27 100: 1/6 duty cycle, 1/3 bias (6 COM X 18/26 SEG) COM: COM0-5, SEG: SEG0 -23, COM6-7 shared as SEG26-SEG27 101: 1/6 duty cycle, 1/4 bias (6 COM X 18/26 SEG) COM port: COM0-5 SEG port: SEG0-23, COM6-7 shared as SEG26-SEG27 Others: 1/4 duty cycle, 1/3 bias (4 COM X 16/24 SEG) COM: COM0-3, SEG: SEG0-23
2	DPSEL	LCD, LED selection control bit 0: Select LCD driver, LED driver is invalid 1: Select LED driver, LCD driver is invalid
1	SCAN_MODE	LCD, LED scan mode configuration 1: Cycle scan mode 0: Interrupt scan mode
0	COM_MOD	High current sink IO port drive enable 1: As a high current sink IO port; 0: Can be configured for other functions;

		When used as a high current sink IO port, by configuring the GPIO register to output the drive timing, the LED/LCD scan configuration is invalid

15.3.3.3. LCD Mode Register

DP_MODE (B2H) LCD, LED mode register

Bit number	7	6	5	4	3	2	1	0
Symbol	LED_MOD	LCD_CKSEL		LCD_RSEL	LCD_FCSEL		LCD_RMOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
6~5	LCD_CKSEL	LCD clock selection register 10/11: Select RC1M 01: Select XTAL 32768Hz 00: Select LIRC
3~2	LCD_FCSEL	Charge time control bit 00: 1/8 LCD com period; 01: 1/16 LCD com period; 10: 1/32 LCD com period; 11: 1/64 LCD com period
4	LCD_RSEL	LCD bias resistance selection control bit 0: The sum of LCD bias resistance is 225k; 1: The sum of LCD bias resistance is 900k
1~0	LCD_RMOD	Drive mode selection bit 00: Traditional resistance mode (slow charging mode), the total bias resistance is 225k/900k, when LCD_RSEL = 0, the total LCD bias resistance is 225K, when LCD_RSEL = 1, the total LCD bias resistance is 900K 01: Traditional resistance mode (fast charging mode), the total bias resistance is 60k 10/11: Fast and slow charging automatic switching mode, the total bias resistance is automatically switched between 60k and 225k/900k

15.3.3.4. LCD Period Configuration Register

SCAN_WIDTH (B3H) LED period configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							

R/W	R/W
Reset value	0

Bit number	Bit symbol	Description
7~0	--	In LCD drive mode, the corresponding single COM port scan time: period=(scan_width+1)*64us, support the configuration range 0.064~4.096ms, the upper two digits are reserved Note: In this mode, this register is only applicable to the LCD selection clock CLK_1M mode, the slowest LCD frame rate in other clock modes is 64Hz (8*24)

15.3.3.5. LCD Contrast Configuration Register

DP_CON1 (B9H) LCD contrast configuration register

Bit number	7	6	5	4
Symbol	-	TRI_COM_INV	MATRIX_MOD	PD_LCD_POWER
R/W	-	R/W	R/W	R/W
Reset value	-	0	0	0
Bit number	3	2	1	0
Symbol	VOL			
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
4	PD_LCD_POWER	LCD contrast control enable bit 0: Turn off LCD contrast control; 1: Turn on LCD contrast control
3~0	VOL	LCD contrast control bit 0000: VLCD = 0.53VDD; 0001: VLCD = 0.56VDD; 0010: VLCD = 0.59VDD; 0011: VLCD = 0.63VDD; 0100: VLCD = 0.66VDD; 0101: VLCD = 0.69VDD; 0110: VLCD = 0.72VDD; 0111: VLCD = 0.75VDD; 1000: VLCD = 0.78VDD; 1001: VLCD = 0.81VDD; 1010: VLCD = 0.84VDD; 1011: VLCD = 0.88VDD; 1100: VLCD = 0.91VDD; 1101: VLCD = 0.94VDD; 1110: VLCD = 0.97VDD; 1111: VLCD = 1.00VDD

15.3.3.6. Interrupt Status Register

INT_PE_STAT (AEH) Interrupt status register

Bit number	7	6	5	4
Symbol	INT_PWM1_STAT	INT_TIMER3_STAT	INT08_STAT	INT_WDT_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0
Bit number	3	2	1	0
Symbol	INT_TIMER2_STAT	INT_PWM0_STAT	INT_LCD_STAT	INT_LED_STAT
R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0

Bit number	Bit symbol	Description
1	INT_LCD_STAT	LCD interrupt status mark, this bit is cleared by writing 0, and it can also be cleared by writing SCAN_START 1: Interrupt is valid; 0: Interrupt is invalid

IEN1 (E6H) Interrupt enable register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	EX7	EX6	-	EX4	EX3	EX2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	EX6	LED/LCD interrupt enable 1: LED/LCD interrupt enable; 0: LED/LCD interrupt disable

IRCON1 (F1H) Interrupt flag register 1

Bit number	7	6	5	4	3	2	1	0
Symbol	IE7	IE6	-	IE4	IE3	IE2	-	-
R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IE6	LED/LCD interrupt flag 1: LED/LCD interrupt flag 0: Clear LED/LCD interrupt flag

IPL1 (F6H) Interrupt priority register1

Bit number	7	6	5	4	3	2	1	0
Symbol	IPL1.7	IPL1.6	-	IPL1.4	IPL1.3	IPL1.2	-	-

R/W	R/W	R/W	-	R/W	R/W	R/W	-	-
Reset value	0	0	-	0	0	0	-	-

Bit number	Bit symbol	Description
6	IPL1.6	LED/LCD interrupt priority bit 1: LED/LCD interrupt is high priority; 0: LED/LCD interrupt is low priority

15.3.4. LCD Secondary Bus Register

15.3.4.1. LCD_SEG Port Selection Configuration Register

LCD_IO_SEL_1 (1FH) LCD_SEG0-7 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG0-7 port selection configuration register. A Bit of 1 indicates that SEG port function is selected. 1: Select SEGMENT port mode; 0: Select IO port mode

LCD_IO_SEL_2 (20H) LCD_SEG8-15 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG8-15 port selection configuration register. A Bit of 1 indicates that SEG port function is selected. 1: Select SEGMENT port mode; 0: Select IO port mode

LCD_IO_SEL_3 (21H) LCD_SEG16-23 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit number	Bit symbol	Description
7~0	--	LCD_SEG16-23 port selection configuration register. A Bit of 1 indicates that SEG port function is selected. 1: Select SEGMENT port mode; 0: Select IO port mode

LCD_IO_SEL_4 (22H) LCD_SEG24-27 port selection configuration register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	SEG27/COM7	SEG26/COM6	SEG25/COM5	SEG24/COM4
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset value	-	-	-	-	0	0	0	0

Bit number	Bit symbol	Description
3~0	--	LCD_SEG24-27 port selection configuration register, reserved in non-sharing mode, shared mode COM4~COM7 is LCD_SEG24-27 1: Select SEG24~SEG27 port/COM3~COM7; 0: Select IO port mode

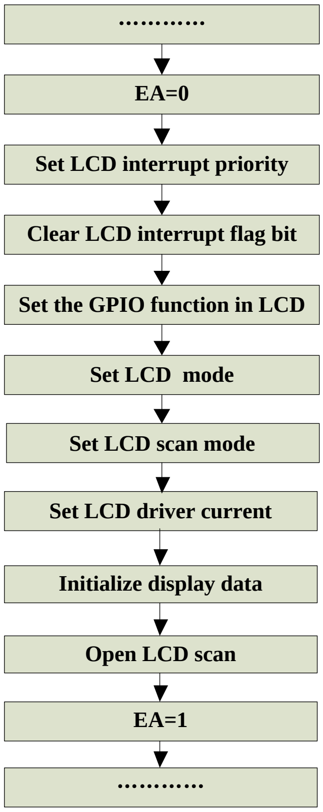
15.3.4.2. Crystal Frequency Selection Register

XTAL_CLK_SEL (63H) Crystal frequency selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	Crystal frequency selection register 1: Select 4MHz; 0: Select 32768Hz

15.3.5. LCD Configuration Process



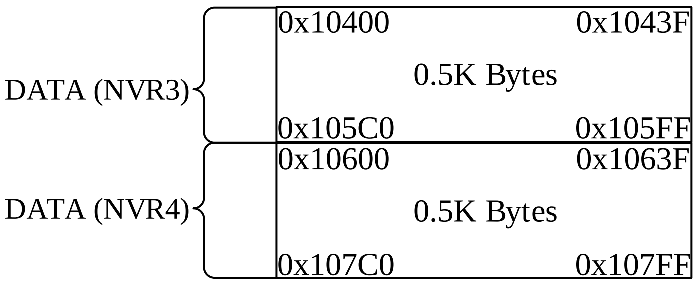
LCD configure process

16. DATA Area

When EEP_SELECT = 0, select address 0xFC00~0xFFFF as DATA area, one page. When using, it needs to perform page erasing, and then perform byte write operation, which can only be written once after erasing. The data area is erased and the data is 0xff.

{SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]}The logical address (0~1023) corresponds to the physical address (0xFC00~0xFFFF).

When EEP_SELECT = 1, select NVR3 and NVR4 as the DATA area, each block of 512Bytes is a page, and the address is (0x10400~0x107FF). When using, it needs to perform page erasing, and then perform byte write operation, which can only be written once after erasing.



NVR3:

{SPROG_ADDR_H[0], SPROG_ADDR_L}The logical address (0x4400+(0~511)) corresponds to the physical address (0x10400~0x105FF.

NVR4:

{SPROG_ADDR_H[0], SPROG_ADDR_L}The logical address (0x4600+(0~511)) corresponds to the physical address (0x10600~0x107FF).

16.1. Page Erase Step

When EEP_SELECT = 0, select the address (0xFC00~0xFFFF) as the DATA area, 1 page.
When EEP_SELECT = 1, select NVR3/4 as DATA area, NVR3 is 1 page, NVR4 is 1 page.

1. SPROG_TIM[4:0] = 0~9 (suggest 5ms), byte write time is fixed at 23.5us, The main() program function is only configured once.
2. Close interrupt
3. EEP_SELECT select;
4. Configure SPROG_ADDR_H, SPROG_ADDR_L, select to erase the page;
5. Configure SPROG_CMD = 0x96;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after erasing is completed;
8. Need to continue to erase data, jump to step 2;
9. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings.

16.2. Byte Write Step

When EEP_SELECT = 0, select the address (0xFC00~0xFFFF) as the DATA area, 1 page.
When EEP_SELECT = 1, select NVR3/4 as DATA area, NVR3 is 1 page, NVR4 is 1 page.

1. SPROG_TIM[4:0] = 0~9(suggest 5ms), byte write time is fixed at 23.5us, The main() program function is only configured once;
2. Close interrupt;
3. EEP_SELECT select;
4. Configure SPROG_ADDR_H, SPROG_ADDR_L, byte write address;
5. Configure SPROG_DATA ;
6. Configure SPROG_CMD = 0x69;
7. Write 4 NOP instructions;
8. Start writing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after completion;
9. Need to continue to write data, jump to step 3;
10. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings.

16.3. Registers

SFR register				
Address	Name	RW	Reset	Description
0xCE	SPROG_ADDR_H	RW	0000_0000b	Address control register
0xCF	SPROG_ADDR_L	RW	0000_0000b	Address control register low 8 bits
0xD1	SPROG_DATA	RW	0000_0000b	Write data register
0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD3	SPROG_TIM	RW	1101_1101b	Erase time control register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x5B	EEP_SELECT	RW	xxxx_xxx0b	DATA area selection register

16.3.1. Address control register

SPROG_ADDR_H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In non-Flash_Boot upgrade mode: Bit[6:2]: DATA area (0xFC00~0xFFFF) selection enable 00000: Select DATA area (0xFC00~0xFFFF), 1024Bytes Other: invalid **1. DATA area (0xFC00~0xFFFF):** config {SPROG_ADDR_H[1:0], SPROG_ADDR_L[7:0]} **2. When SPROG_ADDR_H[2]=1, select NVR4:** config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} **3. When SPROG_ADDR_H[2]=0, select NVR3:** config {SPROG_ADDR_H[0], SPROG_ADDR_L[7:0]} Note: In Flash_Boot upgrade mode, { SPROG_ADDR_H, SPROG_ADDR_L} multiplexing all space addresses of CODE

16.3.2. Address control register low 8 bits

SPROG_ADDR_L(CFH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	SPROG_ADDR_L[7:0]							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	SPROG_ADDR_L[7:0]	The lower 8 bits of the address

16.3.3. Write Data Register

SPROG_DATA(D1H) Write data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							
Bit number	Bit symbol	Description						
7~0	--	data to be written						

16.3.4. Command Register

SPROG_CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Write 0x96: page erase Write 0x69: byte burn Write 0x88: read data indirectly; When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9A, enter the Flash Boot upgrade mode; When continuously writing data 0xFE, 0xDC, 0xBA, 0x98, 0x76, exit the Flash Boot upgrade mode When CFG_BOOT_SEL = 3 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered.

16.3.5. Erase Time Control Register

SPROG_TIM(D3H) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	1	1	1	0	1

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Byte write fixed time is 23.5us
4~0	SPROG_TIM[4:0]	Erase time configuration SPROG_TIM[4:0]=0~31 When the selected address is 0xFC00~0xFFFF: When SPROG_TIM[4:0]=0~9, Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms) When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9, Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time=4.57(ms)

16.3.6. Secondary Bus Register

EEP_SELECT (5BH) DATA area selection register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	R/W
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	--	1: Select NVR3 and NVR4 as DATA area When SPROG_ADDR_H[2]=1, select NVR4; When SPROG_ADDR_H[2]=0, select NVR3 0: Select address (0xFC00~0xFFFF) as DATA area, 1 page

16.4. DATA Area Read

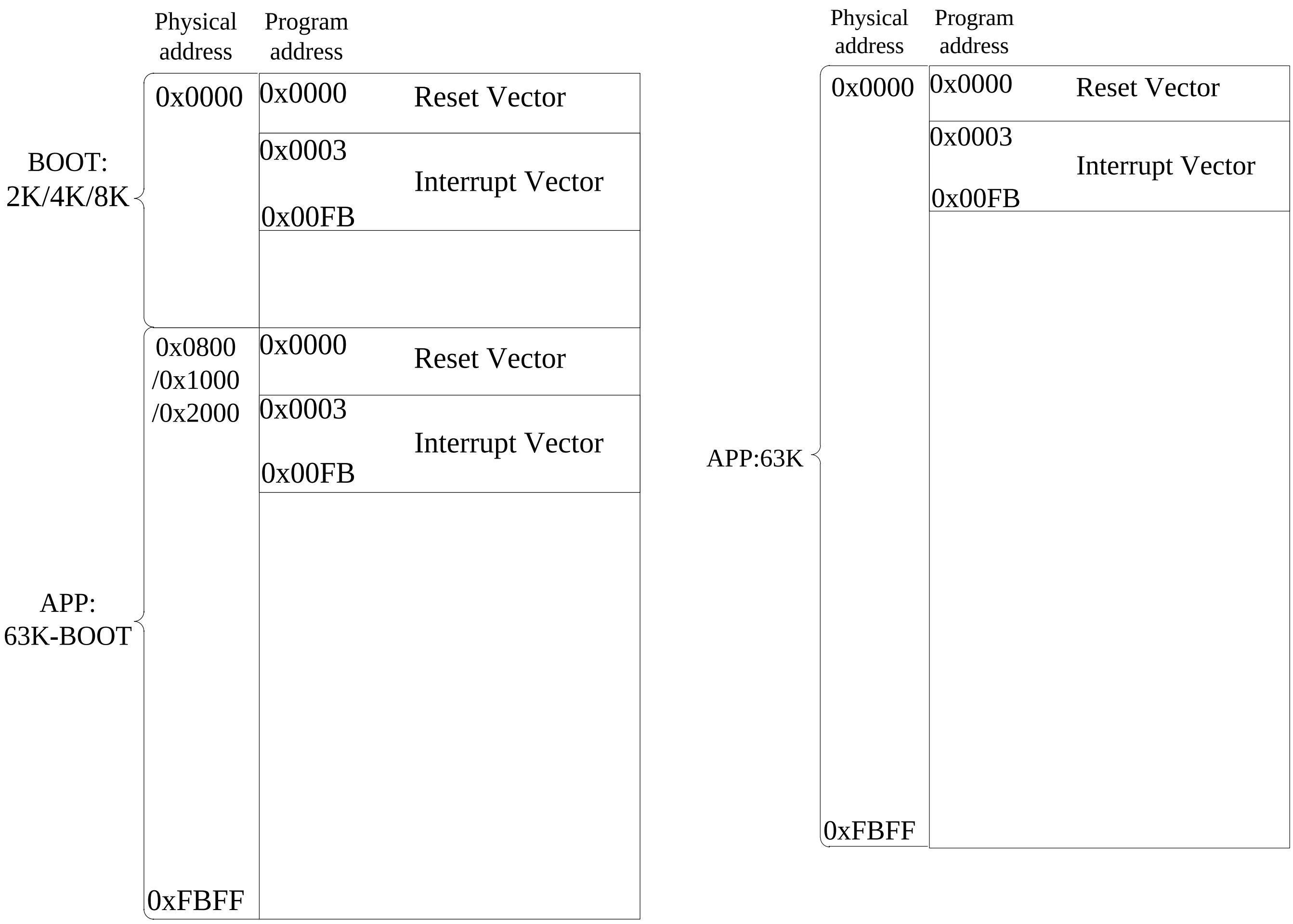
DATA area (0xFC00~0xFFFF) read: directly read the CODE absolute address (0xFC00+0~1023).

NVR3 and NVR4 read:

1. Turn off the interrupt;
2. Configure SPROG_CMD = 0x88;
3. Configure SPROG_ADDR_H, SPROG_ADDR_L, the address to be read;
4. NVR3: {SPROG_ADDR_H, SPROG_ADDR_L} The logical address (0x4400+(0~511)) corresponds to the physical address (0x10400~0x105FF).
   NVR4: {SPROG_ADDR_H, SPROG_ADDR_L} The logical address (0x4600+(0~511)) corresponds to the physical address (0x10600~0x107FF);
5. Read SPROG_RDATA data;
6. Need to continue to read data, jump to step 2 and 3;
7. After reading SPROG_RDATA data, configure SPROG_CMD = 0x00;
8. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00; restore interrupt settings.

17. IAP Operation

CFG_11: [7:6] When CFG_BOOT_SEL is not equal to 3, Flash supports the IAP BOOT upgrade function, by sending IAP operation commands to realize the jump between the BOOT area and the APP area, BOOT comes with storage and write protection, and the size of the BOOT area is set by the configuration word CFG_11:[7:6]- CFG_BOOT_SEL selection: 0: 2K, 1: 4K, 2: 8K.



Left: BOOT and APP partition map; Right:APP map,not-BOOT map

17.1. Flash IAP Related Registers

SFR register				
Address	**Name**	**RW**	**Reset**	**Description**
0xCE	SPROG_ADDR_H	RW	0000_0000b	Address control register
0xCF	SPROG_ADDR_L	RW	0000_0000b	Address control register low 8 bits
0xD1	SPROG_DATA	RW	0000_0000b	Write data register
0xD2	SPROG_CMD	RW	0000_0000b	Command register
0xD3	SPROG_TIM	RW	1101_1101b	Erase time control register

Secondary bus register				
Address	**Name**	**RW**	**Reset**	**Description**
0x5A	FLASH_BOOT_EN	R	xxxx_xxx0b	BOOT mode status selection register
0x5B	EEP_SELECT	RW	xxxx_xxx0b	DATA area selection register
0x6A	BOOT_CMD	RW	0000_0000b	Program space jump instruction register
0x6B	ROM_OFFSET_L	R	0000_0000b	CODE area address offset,low 8bits
0x6C	ROM_OFFSET_H	R	0000_0000b	CODE area address offset,high 8bits

17.1.1. Flash IAP Address Register

SPROG_ADDR_H (CEH) Address control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	In Flash_Boot upgrade mode: {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses of 0x0000~0xFFFF.

SPROG_ADDR_L(CFH) Address control register low 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	The lower 8 bits of the address

17.1.2. Write Data Register

SPROG_DATA(D1H)Write data register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	data to be written

17.1.3. Command Register

SPROG_CMD(D2H) Command register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	When continuously writing data 0x12, 0x34, 0x56, 0x78, 0x9A, enter the Flash Boot upgrade mode; When continuously writing data 0xFE, 0xDC, 0xBA, 0x98, 0x76, exit the Flash Boot upgrade mode When CFG_BOOT_SEL = 3 or the program is running in a non-BOOT space, the BOOT upgrade mode cannot be entered.

17.1.4. Erase Time Control Register

SPROG_TIM(D3H) Erase time control register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	0	1	1	1	0	1

Bit number	Bit symbol	Description
7~5	SPROG_TIM[7:5]	Byte write fixed time is 23.5us
4~0	SPROG_TIM[4:0]	Erase time configuration SPROG_TIM[4:0]=0~31 When the selected address is 0xFC00~0xFFFF: When SPROG_TIM[4:0]=0~9,

		Erase Time = 1.13 + SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time = 9.13 (ms) When selecting NVR3/4 or BOOT upgrade mode: When SPROG_TIM[4:0]=0~9, Erase Time=0.57+0.5* SPROG_TIM[4:0] (ms); When SPROG_TIM[4:0]=10~31, Erase time=4.57(ms)

17.2. Secondary Bus Register

17.2.1. BOOT mode status register

FLASH_BOOT_EN (5AH) BOOT mode status register

Bit number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	FLASH_BOOT_EN
R/W	-	-	-	-	-	-	-	R
Reset value	-	-	-	-	-	-	-	0

Bit number	Bit symbol	Description
0	FLASH_BOOT_EN	1: Indicates that the Flash BOOT upgrade mode has been entered, 0: indicates that the Flash BOOT upgrade mode has been exited. Note: In Flash BOOT upgrade mode, SPROG_ADDR_H, SPROG_ADDR_L, SPROG_DATA, SPROG_CMD, SPROG_TIM are reused as BOOT upgrade function. {SPROG_ADDR_H, SPROG_ADDR_L} are multiplexed into all Flash space addresses from 0x0000 to 0xFFFF.

17.2.2. Program Space Jump Instruction Register

BOOT_CMD (6AH) Program space jump instruction register

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R/W							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	Configure the program space jump instruction, write 5 groups of data (0xFF, 0x00, 0x88, 0x55, 0xAA)

		continuously, jump into the main program space; write 5 groups of data (0x37, 0xC8, 0x42, 0x9A, 0x65), Jump into the Boot program space; the value read out is the byte written recently.

17.2.3. CODE Area Address Offset

The read value is the actual total address offset.

ROM_OFFSET_L (6BH) CODE area address offset,low 8bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

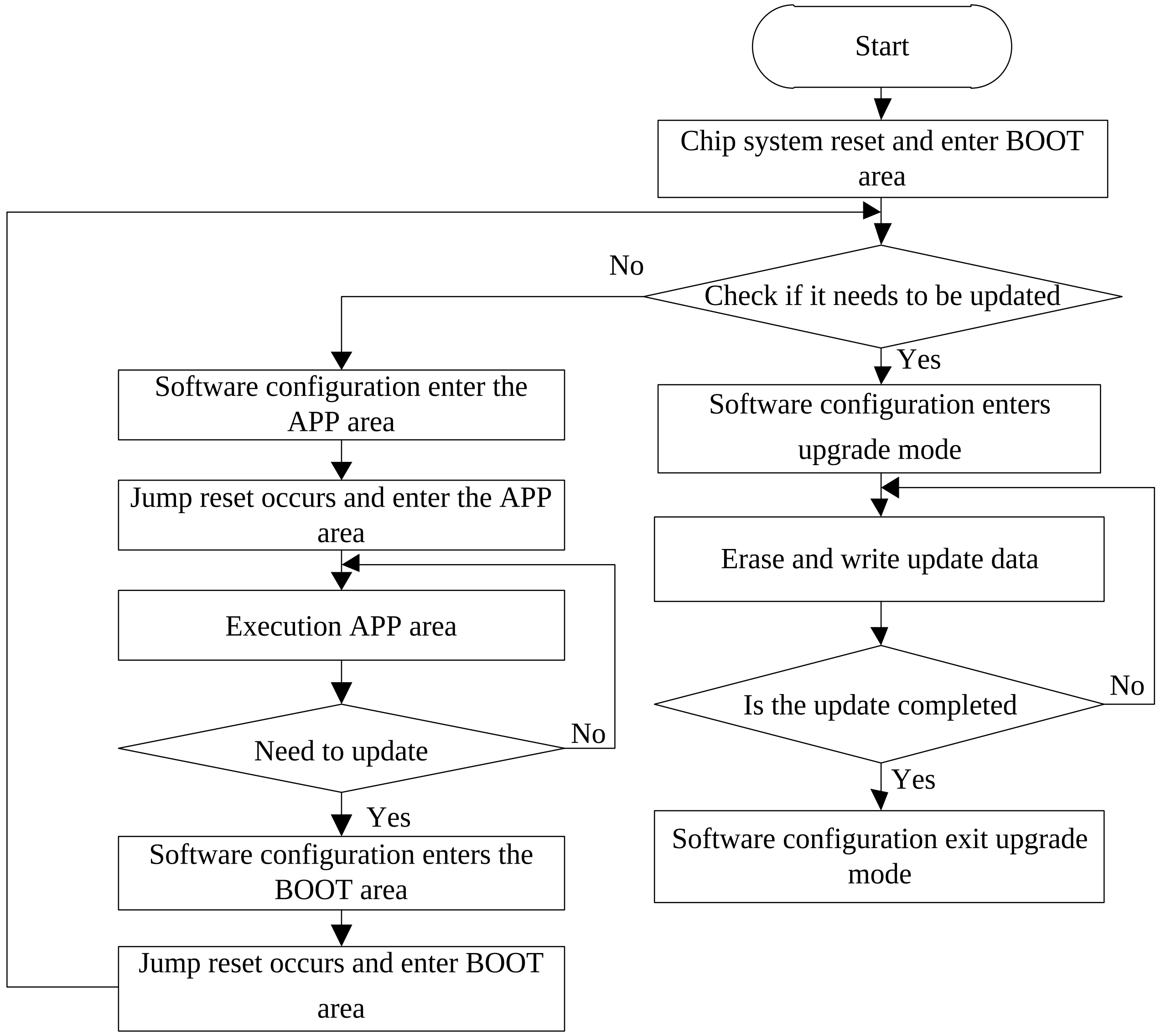
Bit number	Bit symbol	Description
7~0	--	CODE area address offset (low 8bits)

ROM_OFFSET_H (6CH) CODE area address offset, high 8 bits

Bit number	7	6	5	4	3	2	1	0
Symbol	-							
R/W	R							
Reset value	0							

Bit number	Bit symbol	Description
7~0	--	CODE area address offset (high 8bits)

17.3. Flash IAP Operating Procedures



17.3.1. Flash IAP Erase Step

In Flash_BOOT upgrade mode:

1. SPROG_TIM[4:0] = 0~9 (suggest 3ms), the byte write time is fixed at 23.5us, and it is configured only once in the main program main() function initialization;
2. Close interrupt;
3. Configure SPROG_ADDR_L = 0x00;
4. Configure SPROG_ADDR_H([7:1]); select to erase the page;
5. Configure SPROG_CMD = 0x96;
6. Write 4 NOP instructions;
7. Start erasing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after erasing is completed;
8. Need to continue erasing data, jump to step 2;
9. Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings.

17.3.2. Flash IAP Byte Write Step

1. SPROG_TIM[4:0] = 0~9 (suggest 3ms), the byte write time is fixed at 23.5us, and it is configured only once in the main program main() function initialization;
2. Close the interrupt;
3. Configure SPROG_ADDR_H, SPROG_ADDR_L, byte write address;
4. Configure SPROG_DATA;
5. Configure SPROG_CMD = 0x69;
6. Write 4 NOP instructions;
7. Start writing, the CPU turns off the clock f_{SYS}, and turns on the clock f_{SYS} after completion;
8. Need to continue writing data, jump to step 2;

   Configure SPROG_ADDR_L=0x00, SPROG_ADDR_H=0x00, restore interrupt settings;

17.3.3. Flash IAP Operation Instruction

Instruction	Instruction response status	Instruction data
Enter upgrade mode instruction	FLASH_BOOT_EN = 1	0x12, 0x34, 0x56, 0x78, 0x9A
Exit upgrade mode instruction	FLASH_BOOT_EN = 0	0xFE, 0xDC, 0xBA, 0x98, 0x76
Enter the APP area instruction	ROM_OFFSETH/L	0xFF, 0x00, 0x88, 0x55, 0xAA
Enter the BOOT area instruction	ROM_OFFSETH/L	0x37, 0xC8, 0x42, 0x9A, 0x65

Instructions for operation:

1. Enter upgrade mode instruction: SPROG_CMD sequential write: 0x12, 0x34, 0x56, 0x78, 0x9A;
2. Exit upgrade mode instruction: SPROG_CMD sequential write: 0xFE, 0xDC, 0xBA, 0x98, 0x76;
3. Enter the APP area instruction: BOOT_CMD sequential write: 0xFF, 0x00, 0x88, 0x55, 0xAA;
4. Enter the BOOT area instruction: BOOT_CMD sequential write: 0x37, 0xC8, 0x42, 0x9A, 0x65;

Instructions response status:

FLASH_BOOT_EN = 1: Indicates that it has entered Flash BOOT upgrade mode,

FLASH_BOOT_EN = 0: Indicates that the Flash BOOT upgrade mode has been exited

OM_OFFSETH/L address offset status**:**

CFG_BOOT_SEL = 3, ROM_OFFSETH/L = 0x0000// No BOOT upgrade function

CFG_BOOT_SEL != 3, If you are currently in the APP area:

CFG_BOOT_SEL = 0, ROM_OFFSETH/L = 0x0800,

CFG_BOOT_SEL = 1, ROM_OFFSETH/L = 0x1000,

CFG_BOOT_SEL = 2, ROM_OFFSETH/L = 0x2000.

If you are currently in the boot area:

CFG_BOOT_SEL = 0, ROM_OFFSETH/L = 0x0000.

Physical address of program execution = PC + ROM_OFFSETH/L.

Notes:

1. When writing SPROG_CMD, BOOT_CMD instruction data, it must be written in order, otherwise it needs to be written again.
2. The working voltage of MCU is 2.7V~5.5V, and the MCU may work abnormally at 1.5V~2.7V, resulting in abnormal update and misoperation. Therefore, it is recommended not to perform IAP operation when the ADC or LVDT detection voltage is lower than 2.7V before IAP operation .
3. It is recommended to shield the interrupt during the update process to ensure that the IAP operation will not be affected by the interruption, and resume the interruption after the IAP operation is completed, and perform data verification after updating the data to ensure that the data is updated correctly.

17.3.4. Address Correspondence In BOOT Upgrade Mode

Address correspondence in BOOT upgrade mode				
SPROG_ADDR_H[7:1]	Block	Byte write physical address corresponding range (HEX)		
4	4	00000800	--->	000009FF
5	5	00000A00	--->	00000BFF
6	6	00000C00	--->	00000DFF
7	7	00000E00	--->	00000FFF
8	8	00001000	--->	000011FF
9	9	00001200	--->	000013FF
10	10	00001400	--->	000015FF
11	11	00001600	--->	000017FF
12	12	00001800	--->	000019FF
13	13	00001A00	--->	00001BFF
14	14	00001C00	--->	00001DFF
15	15	00001E00	--->	00001FFF
16	16	00002000	--->	000021FF
17	17	00002200	--->	000023FF
18	18	00002400	--->	000025FF
19	19	00002600	--->	000027FF
20	20	00002800	--->	000029FF
21	21	00002A00	--->	00002BFF
22	22	00002C00	--->	00002DFF
23	23	00002E00	--->	00002FFF
24	24	00003000	--->	000031FF
25	25	00003200	--->	000033FF
26	26	00003400	--->	000035FF
27	27	00003600	--->	000037FF
28	28	00003800	--->	000039FF
29	29	00003A00	--->	00003BFF
30	30	00003C00	--->	00003DFF
31	31	00003E00	--->	00003FFF
32	32	00004000	--->	000041FF
33	33	00004200	--->	000043FF
34	34	00004400	--->	000045FF
35	35	00004600	--->	000047FF
36	36	00004800	--->	000049FF
37	37	00004A00	--->	00004BFF

38	38	00004C00	--->	00004DFF
39	39	00004E00	--->	00004FFF
40	40	00005000	--->	000051FF
41	41	00005200	--->	000053FF
42	42	00005400	--->	000055FF
43	43	00005600	--->	000057FF
44	44	00005800	--->	000059FF
45	45	00005A00	--->	00005BFF
46	46	00005C00	--->	00005DFF
47	47	00005E00	--->	00005FFF
48	48	00006000	--->	000061FF
49	49	00006200	--->	000063FF
50	50	00006400	--->	000065FF
51	51	00006600	--->	000067FF
52	52	00006800	--->	000069FF
53	53	00006A00	--->	00006BFF
54	54	00006C00	--->	00006DFF
55	55	00006E00	--->	00006FFF
56	56	00007000	--->	000071FF
57	57	00007200	--->	000073FF
58	58	00007400	--->	000075FF
59	59	00007600	--->	000077FF
60	60	00007800	--->	000079FF
61	61	00007A00	--->	00007BFF
62	62	00007C00	--->	00007DFF
63	63	00007E00	--->	00007FFF
64	64	00008000	--->	000081FF
65	65	00008200	--->	000083FF
66	66	00008400	--->	000085FF
67	67	00008600	--->	000087FF
68	68	00008800	--->	000089FF
69	69	00008A00	--->	00008BFF
70	70	00008C00	--->	00008DFF
71	71	00008E00	--->	00008FFF
72	72	00009000	--->	000091FF
73	73	00009200	--->	000093FF
74	74	00009400	--->	000095FF
75	75	00009600	--->	000097FF

76	76	00009800	--->	000099FF
77	77	00009A00	--->	00009BFF
78	78	00009C00	--->	00009DFF
79	79	00009E00	--->	00009FFF
80	80	0000A000	--->	0000A1FF
81	81	0000A200	--->	0000A3FF
82	82	0000A400	--->	0000A5FF
83	83	0000A600	--->	0000A7FF
84	84	0000A800	--->	0000A9FF
85	85	0000AA00	--->	0000ABFF
86	86	0000AC00	--->	0000ADFF
87	87	0000AE00	--->	0000AFFF
88	88	0000B000	--->	0000B1FF
89	89	0000B200	--->	0000B3FF
90	90	0000B400	--->	0000B5FF
91	91	0000B600	--->	0000B7FF
92	92	0000B800	--->	0000B9FF
93	93	0000BA00	--->	0000BBFF
94	94	0000BC00	--->	0000BDFF
95	95	0000BE00	--->	0000BFFF
96	96	0000C000	--->	0000C1FF
97	97	0000C200	--->	0000C3FF
98	98	0000C400	--->	0000C5FF
99	99	0000C600	--->	0000C7FF
100	100	0000C800	--->	0000C9FF
101	101	0000CA00	--->	0000CBFF
102	102	0000CC00	--->	0000CDFF
103	103	0000CE00	--->	0000CFFF
104	104	0000D000	--->	0000D1FF
105	105	0000D200	--->	0000D3FF
106	106	0000D400	--->	0000D5FF
107	107	0000D600	--->	0000D7FF
108	108	0000D800	--->	0000D9FF
109	109	0000DA00	--->	0000DBFF
110	110	0000DC00	--->	0000DDFF
111	111	0000DE00	--->	0000DFFF
112	112	0000E000	--->	0000E1FF
113	113	0000E200	--->	0000E3FF

114	114	0000E400	--->	0000E5FF
115	115	0000E600	--->	0000E7FF
116	116	0000E800	--->	0000E9FF
117	117	0000EA00	--->	0000EBFF
118	118	0000EC00	--->	0000EDFF
119	119	0000EE00	--->	0000EFFF
120	120	0000F000	--->	0000F1FF
121	121	0000F200	--->	0000F3FF
122	122	0000F400	--->	0000F5FF
123	123	0000F600	--->	0000F7FF
124	124	0000F800	--->	0000F9FF
125	125	0000FA00	--->	0000FBFF

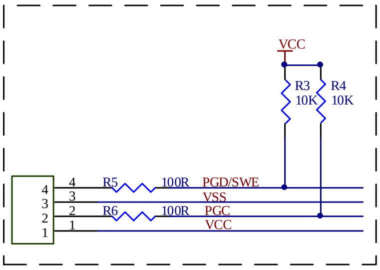
Notes:

1. Byte write physical address corresponding register: {SPROG_ADDR_H[7:0], SPROG_ADDR_L[7:0]};
2. 512 Bytes per Block;
3. When operating the 2K/4K/8K Block in the area where the BOOT is located, the BOOT is write-protected and the operation is invalid.
4. When the BOOT function is used, the absolute address of all CODE areas of the program needs to be subtracted from the offset address of ROM_OFFSET_H/L (PC - ROM_OFFSET), and then the absolute address of the CODE area is accessed.

18. Burning and Debugging

18.1. SWE Circuit Connection

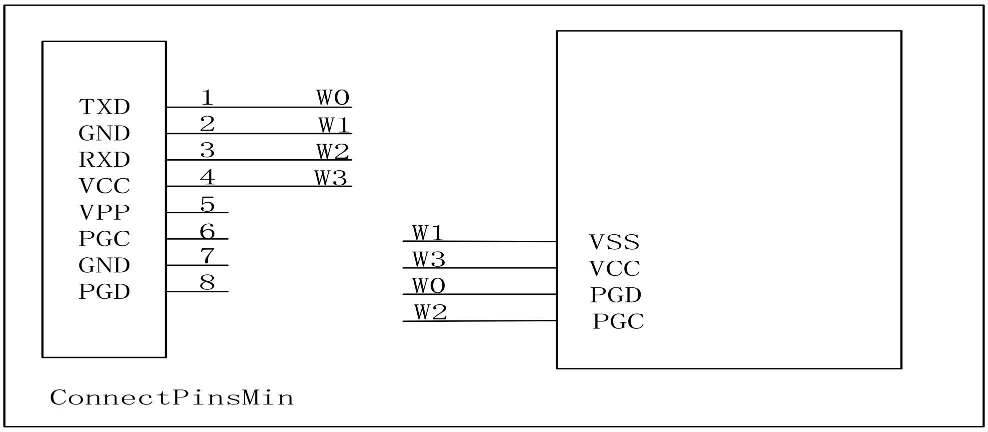
Two-wire programming and single-wire debugging. When performing simulation debugging, you need to connect a SWE wire. In the SWE debugging mode, the IO function of the SWE port is blocked. It is recommended not to configure other functions of the SWE debugging IO port to avoid affecting the SWE debugging function.



SWE circuit connection reference diagram

18.2. Burning and Debugging

Connect the chip PGC, PGD, VCC, VSS four lines. When entering the programming interface, select the chip of the corresponding model. Open the compiled HEX file, click on a built-in flash to wait for burning.



19. CPU Instruction System

19.1. Instruction Code

The BF7515CM44-LJTX instructions are divided into signal-byte instructions, double-byte instructions and three-byte instructions.

Signal-byte instructions: A signal-byte instruction consists of 8 bit binary code. There are only instruction opcodes in the instruction, no instruction operand or instruction operand is implied in the instruction opcode. There are 49 such instructions.

Double-byte instructions: Consists of two bytes, one for opcode and the other for the operand (or operand address), stored in order in program memory. There are 46 such instructions.

Three-byte instructions: Consists of one byte of instruction opcode and two bytes of operands (or operand address). There are 16 such instructions.

19.2. Instruction Set

In order to describe the instructions conveniently, some symbols are used in the instructions. The meanings of these symbols are as follows:

Addr 11	Low 11 bit address
addr 16	16 bit address
direct	Direct addressing, 8 bit internal data and address(including SFR)
bit	Bit address
#data	8 bit immediate
#data16	16 bit immediate
rel	Signed 8 bit relative displacement
n	Number 0~7
Rn	R0~R7 working register of the current register bank
i	Number 0, 1
Ri	working register R0, R1
@	Register indirect addressing
←	Data transfer direction
∧	Logic ‘and’
∨	Logic ‘or’
⊕	Logic ‘xor’
√	Have an effect on the flag
×	No effect on the flag

CPU instruction symbol table

Provides the assembly instructions used, the function of each instruction, the number of bytes occupied, the execution cycle of the instruction, and the effect on the corresponding flags:

8 bit data transfer instructiion								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
MOV A	Rn	A←(Rn)	√	×	×	×	1	1
	direct	A←(direct)	√	×	×	×	2	1
	@Ri	A←((Ri))	√	×	×	×	1	1
	#data	A←data	√	×	×	×	2	1
MOV Rn	A	Rn←(A)	×	×	×	×	1	1
	direct	Rn←(direct)	×	×	×	×	2	2
	#data	Rn←data	×	×	×	×	2	1
MOV direct1	A	direct1←(A)	×	×	×	×	2	1
	Rn	direct1←(Rn)	×	×	×	×	2	1
	direct2	direct1←(direct2)	×	×	×	×	3	2
MOV direct	@Ri	direct←((Ri))	×	×	×	×	2	2
	#data	direct←data	×	×	×	×	3	1

MOV @Ri	A	(Ri)←(A)	×	×	×	×	1	1
	direct	(Ri)←(direct)	×	×	×	×	2	2
	#data	(Ri)←data	×	×	×	×	2	1
16 bit data transfer instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
MOV DPTR,#data16		DPTR←data16		×	×	×	3	1
External data transfer and table lookup instructions								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
MOVX @DPTR,A		(DPTR)←(A)	×	×	×	×	1	1
MOVC A,	@A+DPTR	A←((A)+(DPTR))	√	×	×	×	1	1
	@A+PC	A←((A)+(PC))	√	×	×	×	1	1
MOVX A,	@DPTR	A←(DPTR)	√	×	×	×	1	1
Notes: The number of cycles and the number of bytes of the MOVX instruction can be configured through registers CKCON<2:0>.								
Exchange class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
XCH A,	Rn	(Rn)←(A)	√	×	×	×	1	1
	direct	(A)←(direct)	√	×	×	×	2	2
	@Ri	(A)←((Ri))	×	×	×	×	1	2
XCHD A,@Ri		(A)3~0~((Ri))3~0	√	×	×	×	1	2
SWAP A		(A)7-4~(A)3-0	√	×	×	×	1	1
Arithmetic operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
ADD A,	Rn	A←(A)+(Rn)	√	√	√	√	1	1
	direct	A←(A)+(direct)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri))	√	√	√	√	1	2
	#data	A←(A)+data	√	√	√	√	2	1
ADDC A,	Rn	A←(A)+(Rn)+(C)	√	√	√	√	1	1
	direct	A←(A)+(direct) +(C)	√	√	√	√	2	2
	@Ri	A←(A)+((Ri)) +(C)	√	√	√	√	1	2
	#data	A←(A)+data+(C)	√	√	√	√	2	1
INC	A	A←(A)+1	√	×	×	×	1	1
	Rn	Rn←(Rn)+1	×	×	×	×	1	1
	direct	direct←(direct)+1	×	×	×	×	2	2

	@Ri	(Ri)←((Ri))+1	×	×	×	×	1	2
	DPTR	DPTR←((DPTR))+1	×	×	×	×	1	2
DA A		BCD code adjustment	√	×	√	√	1	1
SUBB A	Rn	A←(A)-(Rn)-(C)	√	×	×	×	1	1
	direct	A←(A)-(direct)-(C)	√	√	√	√	2	2
	@Ri	(A)←(A)-((Ri))-(C)	√	√	√	√	1	2
	#data	A←(A)-data-(C)	√	√	√	√	2	1
DEC	A	A←(A)-1	√	×	×	×	1	1
	Rn	Rn←(Rn)-1	×	×	×	×	1	1
	direct	direct←(direct)-1	×	×	×	×	2	2
	@Ri	(Ri)←((Ri))-1	×	×	×	×	1	2
MUL AB		BA←(A)*(B), after performing the multiplication operation, the lower byte is stored in A and the high byte is stored in B.	√	√	×	0	1	1
DIV AB		A←(A)/(B) B←remainder	√	√	×	0	1	1
Notes: When the DA instruction is used, the adjustment rules are as follows: if the low 4 bits of accumulator A are greater than 9 or AC=1, then A←A+06H; if the high 4 bits of accumulator A are greater than 9 or CY=1, then A←A+60H.								
Logical operation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
CLR A		A←00H	√	×	×	×	1	1
CPL A		A←($\overline{A}$)	√	×	×	×	1	1
ANL A,	Rn	A←(A)∧(Rn)	√	×	×	×	1	1
	direct	A←(A)∧(direct)	√	×	×	×	2	2
	@Ri	A←(A)∧((Ri))	√	×	×	×	1	2
	#data	A←(A)∧data	√	×	×	×	2	1
ANL direct,	A	direct←(A)∧(direct)	×	×	×	×	2	2
	#data	direct←(direct)∧data	×	×	×	×	3	2
ORL A,	Rn	A←(A)∨(Rn)	√	×	×	×	1	1
	direct	A←(A)∨(direct)	√	×	×	×	2	2
	@Ri	A←(A)∨((Ri))	√	×	×	×	1	2
	#data	A←(A)∨data	√	×	×	×	2	1
ORL direct,	A	direct←(direct)∨(A)	×	×	×	×	2	2
	#data	direct←(direct)∨data	×	×	×	×	3	2
XRL A,	Rn	A←(A)⊕(Rn)	√	×	×	×	1	1

	direct	A←(A)⊕(direct)	√	×	×	×	2	2
	@Ri	A←(A)⊕((Ri))	√	×	×	×	1	2
	#data	A←(A)⊕data	√	×	×	×	2	1
XRL direct,	A	direct←(direct)⊕(A)	×	×	×	×	2	2
	#data	direct←(direct)⊕data	×	×	×	×	3	2

Loop, shift class instruction

Mnemonic	Function	Impact on the flag				Number of bytes	Cycle number
		P	OV	AC	CY		
RL A	The content in A is rotated left by one bit.	×	×	×	×	1	1
RLC A	A content with carry left shift one bit.	√	×	×	√	1	1
RR A	The content in A is rotated right by one bit.	×	×	×	×	1	1
RRC A	A content with carry right shift one bit.	√	×	×	√	1	1

Call, return class instruction

Mnemonic	Function	Impact on the flag				Number of bytes	Cycle number
		P	OV	AC	CY		
LCALL addr16	(PC)←(PC)+3, (SP)←(PC), (PC)←addr16	×	×	×	×	3	2
ACALL addr11	(PC)←(PC)+2, (SP)←(PC), (PC10~0)←addr11	×	×	×	×	2	2
RET	(PC)←((SP))	×	×	×	×	1	2
RETI	(PC)←((SP)) return from interrupt	×	×	×	×	1	2

Transfer class instruction

Mnemonic	Function	Impact on the flag				Number of bytes	Cycle number
		P	OV	AC	CY		
LJMP addr16	PC←addr15~0	×	×	×	×	3	2
AJMP addr11	PC10~0←addr10~0	×	×	×	×	2	2
SJMP rel	PC←(PC)+rel	×	×	×	×	2	2
JMP @A+DPTR	PC←(A)+(DPTR)	×	×	×	×	1	1
JZ rel	PC←(PC)+2, if(A)=0, PC←(PC)+rel	×	×	×	×	2	2
JNZ rel	PC←(PC)+2, if(A)≠0,	×	×	×	×	2	2

		PC←(PC)+rel						
JC	rel	PC←(PC)+2, if(CY)=1, PC←(PC)+rel	×	×	×	×	2	2
JNC	rel	PC←(PC)+2, if(CY)=0, PC←(PC)+rel	×	×	×	×	2	2
JB	bit,rel	PC←(PC)+3, if(bit)=1, PC←(PC)+rel	×	×	×	×	3	2
JNB	bit,rel	PC←(PC)+3, if(bit)=0, PC←(PC)+rel	×	×	×	×	3	2
JBC	bit,rel	PC←(PC)+3, if(bit)=1, then bit←0, PC←(PC)+rel	×	×	×	×	3	2

CJNE	A, direct,rel	PC←(PC)+3,
		if(A) ≠direct then
		PC(PC)+rel
		if(A)<(direct),thenCY←1
			×	×	×	×	3	2

	A,#data,rel	PC←(PC)+3,
		if(A) ≠data
		then PC(PC)+rel
		if(A)<(data),
		thenCY←1
			×	×	×	×	3	2

	Rn,#data,rel	PC←(PC)+3,
		if(Rn) ≠data
		then
		PC←(PC)+rel
		if(Rn)<(data), then CY←1
			×	×	×	×	3	2

	@Ri,#data,rel	PC←(PC)+3, if((Ri)) ≠data Then PC←(PC)+rel if((Ri))<(data),then CY←1	×	×	×	×	3	2
DJNZ	Rn,rel	PC←(PC)+2,Rn←(Rn)-1, if(Rn) ≠0, then PC←(PC)+rel	×	×	×	×	2	2
	direct,rel	PC←(PC)+3, (direct)←(direct)-1, If (direct)≠0,	×	×	×	×	3	2

		Then PC←(PC)+rel						
Stack, empty operation class instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
PUSH	direct	SP←(SP)+1,(SP)←(direct)	×	×	×	×	2	2
POP	direct	direct←(SP),SP←(SP)-1	×	×	×	×	2	2
NOP		empty operation	×	×	×	×	1	1
Bit manipulation instruction								
Mnemonic		Function	Impact on the flag				Number of bytes	Cycle number
			P	OV	AC	CY		
MOV	C,bit	CY←bit	×	×	×	√		2
	bit,C	bit←CY	×	×	×	×	2	2
CLR	C	CY←0	×	×	×	√	1	1
	bit	bit←0	×	×	×	×	2	2
SETB	C	CY←1	×	×	×	√	1	1
	bit	bit←1	×	×	×	×	2	2
CPL	C	CY←($\overline{CY}$)	×	×	×	√	1	1
	bit	bit←($\overline{bit}$)	×	×	×	×	2	2
ANL	C,bit	C←(C)∧(bit)	×	×	×	√	2	2
	C ,/bit	C←(C)∧($\overline{bit}$)	×	×	×	√	2	2
ORL	C,bit	C←(C)∨(bit)	×	×	×	√	2	2
	C,/bit	C←(C)∨($\overline{bit}$)	×	×	×	√	2	2

Pseudo-instruction		
Mnemonic	Instruction format	Function Description
ORG	【tab:】ORG addr16	Define the first address of tab
EQU	tab EQU data/tab	Assign values to labels
DB	【tab:】 DB item or item tabel	Define a-byte or multi-byte
DW	【tab:】 DW item or item tabel	16 bit word content used to define two or more cells in memory
DS	【tab:】DS expression	Specifies to leave several memory cells starting with the label
BIT	tab BIT address	Assign a bit address to a label
END	END is placed at the end of the assembly language program to tell the assembler that the source program ends here.	

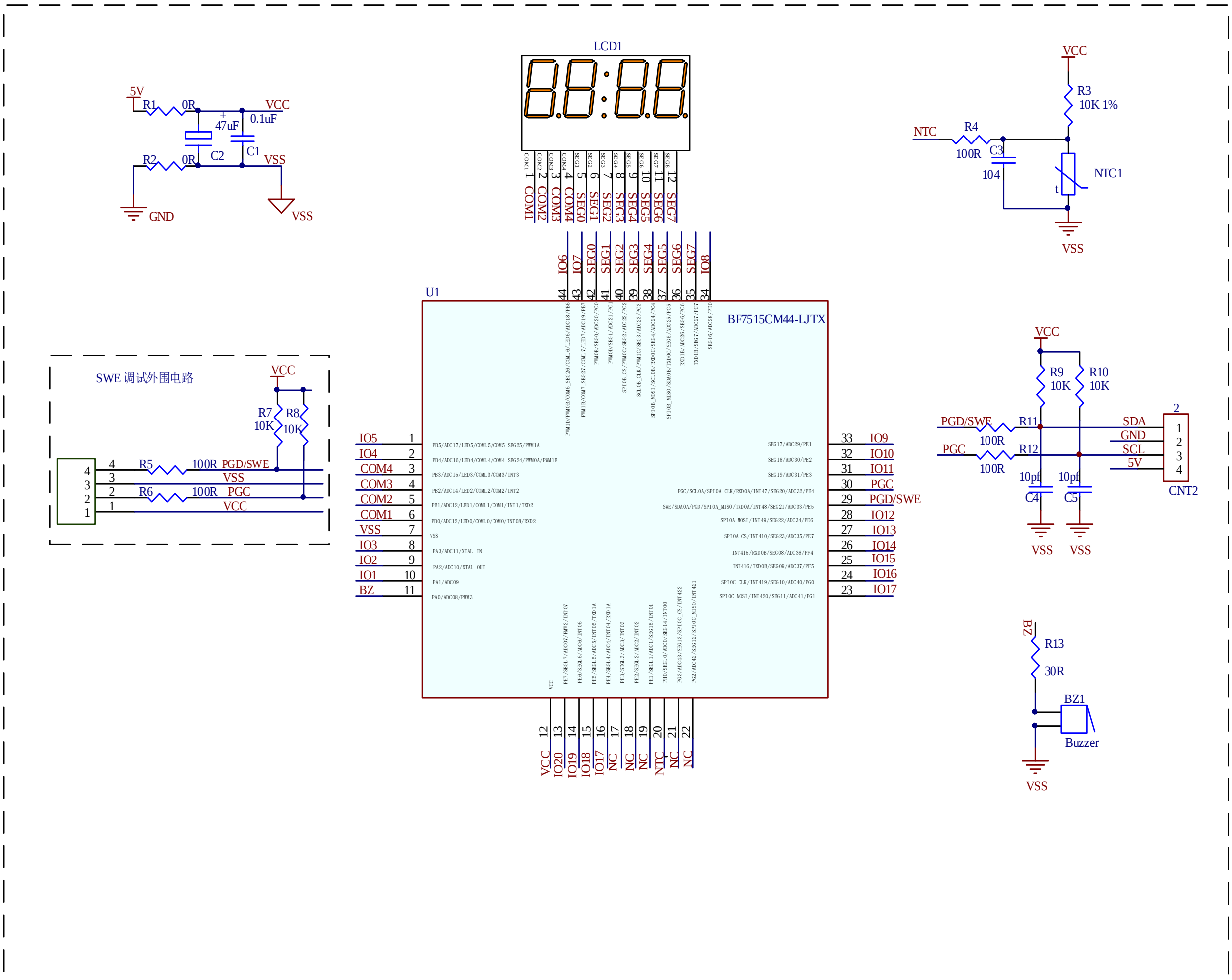
CPU instruction set table

CPU related register

SFR register				
Address	Name	RW	Reset	Description
0x81	SP	RW	0x07	Stack pointer register
0x82	DPL	RW	0x00	Data pointer register 0 low 8 bit
0x83	DPH	RW	0x00	Data pointer register 0 high 8 bit
0x87	PCON	RW	0x00	Idle mode 1 select register
0xE0	ACC	RW	0x00	Accumulator
0xF0	B	RW	0x00	B register

CPU SFR register list

20. Reference Application Circuit

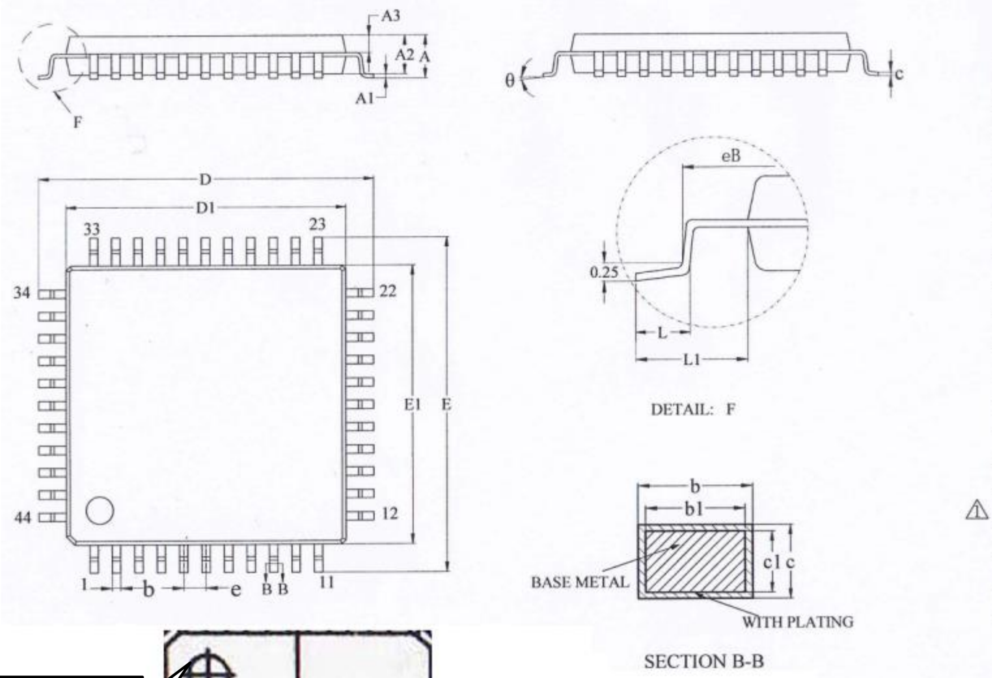


Note: the above reference schematic reference circuit is only for reference design.

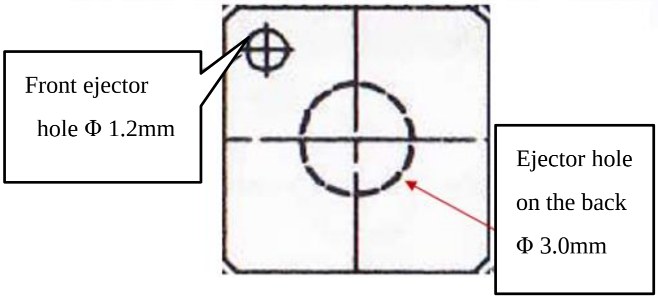
1. **SWE debugging peripheral circuit only SWE adjustment trial, if there is a pull-up resistor on the simulator or adapter board, there is no need to connect the SWE pull-up resistor.**
2. **Replace the 0Ω resistance of the power supply and ground in parallel with magnetic beads. The EMI test item (RE) can increase the test margin. The recommended parameter is 600 Ω@100MHz.**

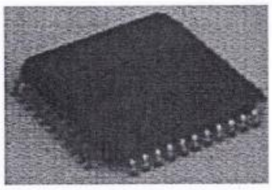
21. Package Information

Tianshui Huatian:

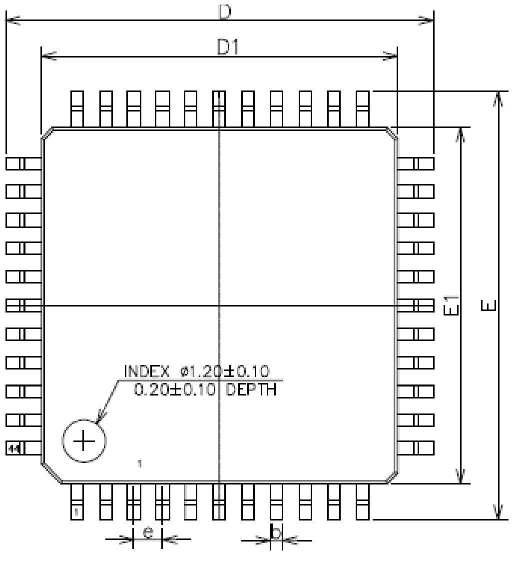


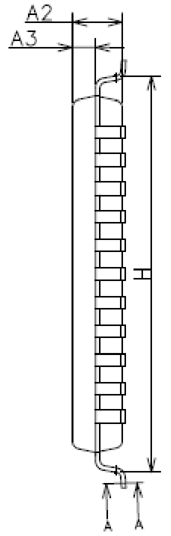
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°



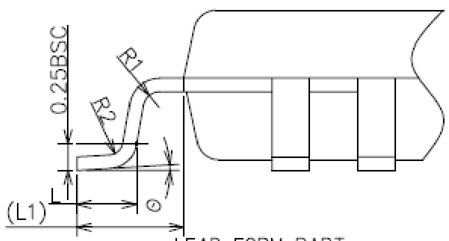


Tongfuwei:

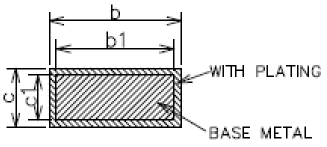




	MILLMETER		
SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.42
b1	0.32	0.35	0.38
c	0.13	—	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.70	0.80	0.90
H	11.09	11.13	11.17
L	0.53	—	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°



LEAD FORM PART

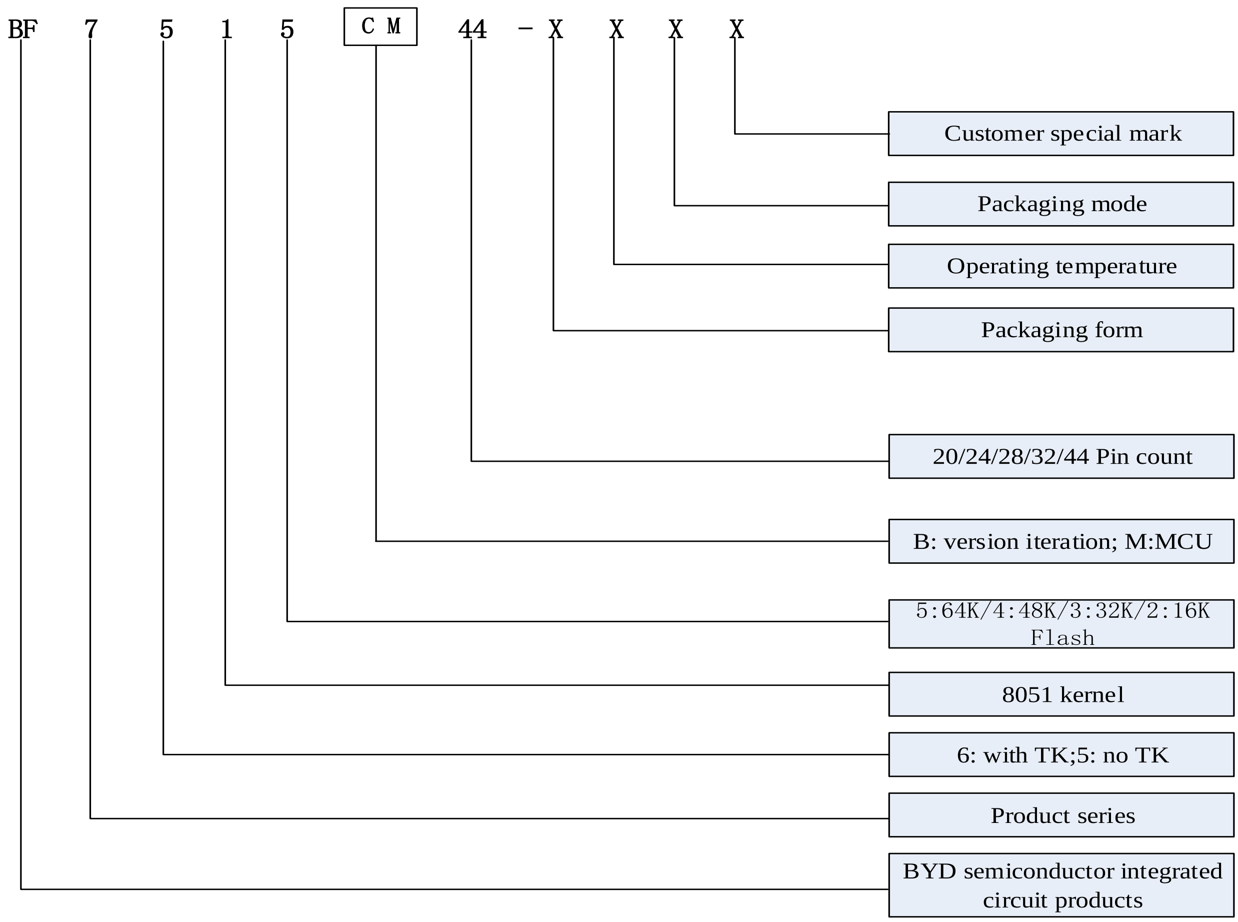


SECTION A—A

Ordering Information

Package	Work temperature		Package style	Keep the follow-up
S: SOP	Car grade	A: -40℃~+150℃	B: tap	-
A: SSOP		B: -40℃~+125℃	L: feed tube	-
T: TSSOP		C: -40℃~+105℃	T: tray	-
M: MSSOP		D: -40℃~+85℃	-	-
L: LQFP	Industrial grade	K: -40℃~+85℃	-	-
Q: QFN		J: -40℃~+105℃	-	-
B: BGA		L: -40℃~+125℃	-	-
D: DIP	Consumer grade	P: -25℃~+70℃	-	-
-		Q: 0℃~+70℃	-	-

Example:



Revision Record

Revision date	Revised content	Reviser	Remarks
2021-12-31	V1.0	JYY	V1.0
2022-01-19	1. Update features 2. Update memory description 3. Update low power current 4. Update clock block diagram 5. Update header	YNN	V1.1
2022-06-07	1. Update the working mode 2. Update the IO structure diagram 3. Update the description of LCD COM*SEG correspondence table 4. Update the LVDT configuration process 5. Update the description of registers 0x58, 0x65, 0xB1	YNN	V1.2
2022-10-25	1. Add limit parameter description 2. Delete the maximum and minimum values of high current in DC characteristics 3. Update the description of "LED dot matrix drive LEDX arrangement order" 4. Update the description of secondary bus register 0x23 5. Add DATA area erase instructions	YNN	V1.3

Disclaimer

1. The information contained herein is subject to change without notice, see the revision record for details. Please contact FAE or the agent for the latest version.
2. BYD Semiconductor Company Limited exerts the greatest possible effort to ensure high quality and reliability. Nonetheless, due to the inherent characteristics of general semiconductor devices such as electrical sensitivity and vulnerability to external physical damage, our products may malfunction or fail under these circumstances. When using our company's products, users are responsible for designing a safe and stable system environment in compliance with safety rules. Users can avoid possible accidents, fires and public injuries by removing redundant devices, failure prevention and fire prevention measures. When the user uses the product, please follow the operating steps specified in the company's latest manual to use the product.
3. The products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). The company's products can not be used in some special equipment that requires extremely high stability and quality, so as to avoid accidents such as casualties. The range of products that cannot be applied includes atomic energy control equipment, aircraft and aviation devices, transportation equipment, traffic signal equipment, combustion control equipment, medical equipment, and all safety equipment. The company shall not be responsible for any loss or injury caused by users who use it within the non-product application ranges listed above.