BS32F103xBx6

DATASHEET

Version: V1.0.1 Date: 24/03/2023

Features

- **72MHz Cortex® -M4F 32-bit CPU**
- **Memories**
  - 128 Kbytes of Flash memory with read and write protection
  - 32 Kbytes of SRAM
- **Power Supply**
  - VDD = 2.5V ~ 5.5V
- **Clock & Crystal Oscillator**
  - External oscillator 32.768kHz
  - High-speed Internal 1M RC
  - Low-speed Internal 32K RC
  - 72M PLL
  - SysClock: 72M/64M/48M
  - IWDG clock source: RC32K
- **Multiple GPIOs**
  - Multiple 5 V-tolerant I/Os
  - All mappable on external interrupt
- **Timer/Counter**
  - One16-bit advanced control timer(TIM1)
  - Three 16-bit general-purpose timer (TIM2,TIM3,TIM4)
  - One 20-bit basic timer (TIM6)
  - Independent watchdog (IWDG)
  - Window watchdog (WWDG)
  - SysTick timer
- **RTC with alarm and calender**
- **Communication interfaces**
  - Up to 3 UART interfaces, independent clock, supporting I/O mapping
  - Up to 2 SPI interfaces with master/slave
  - Up to 2 I2C interfaces with master/slave, supporting fast mode of 1Mb/s
  - CAN standard interfaces supporting 2.0A and 2.0B active modes of CAN protocol
- **32-channel DMA controller with mapping**
- **Two 12-bit, 1.0μs ADC (multiple channels)**
- **CRC calculation unit**
- **Reset**
  - Power-on/Power-down reset (POR/PDR)
  - Watchdog Reset
  - External Pin Reset
  - Flash Soft Reset
  - CPU Soft Reset
  - CPU Lock Reset
  - Shutdown Reset
  - Address Overflow Reset
- **Operating Modes**
  - Active mode (Active)
  - Low-power modes:
    - ❖ Sleep
    - ❖ Sleepdeep
    - ❖ Shutdown
- **Serial Wire Debug (SWD)**
- **Operating Conditions**
  - 2.5V to 5.5V
  - - 40℃ to 85℃
- **Packages**: LQFP48/LQFP64

Part Number

BS32F103CBT6	BS32F103RBT6

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1 Introduction

This datasheet provides the basic information,data parameters,function modules,ordering information and mechanical device characteristics of the BS32F103xBx6 microcontrollers.

The BS32F103x microcontrollers family incorporates the high performance ARM®-Cortex®-M4 RISC operating at a 72MHz frequency,high speed embedded memories(Flash memory up to 128 Kbytes and SRAM up to 32 Kbytes).BS32F103x family includes devices in two different package type:48 pins and 64pins,package type is LQFP48 and LQFP64 forms.All devices offer four 16-bit timers (one advanced-control timer, three general-purpose timers), a 20-bit timer, as well as standard and advanced communication interfaces: up to two I2Cs and SPIs, three UARTs and a CAN .

The BS32F103x microcontrollers family operates from a 2.5V to 5.5V power supply and the working temperatures is -40℃ to 85℃.The devices provides a variety of different operating modes to respond to the power consumption requirements of different situations.

The BS32F103x microcontrollers family suitable for a wide range of applications such as motor drives, application control,medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

2 Features

Table 2.1 BS32F103xBT6 functions and configurations

Peripheral		BS32F103xBT6	
		BS32F103RBT6	BS32F103CBT6
Flash (KB)		128	
SRAM (KB)		32	
Maximum CPU Frequency		72MHz	
GPIO		51	37
EXTI		0 to 15	
Timer	Advanced-control timer (1)	1 (16-bit)	
	General-purpose Timer (2)	3 (16-bit)	
	Basic Timer(3)	1 (20-bit)	
Communication Interfaces	SPI	2	
	I2C	2	
	UART	3	
	CAN	1	
12-bit ADC (numbers of channel)		Two 18 channels (16 external input channels + 1 internal reference voltage channel + 1 internal temperature sensor channel)ADC	Two 12 channels (10 external input channels + 1 internal reference voltage channel + 1 internal temperature sensor channel)ADC
DMA		Single AHB master, 32 independently configurable channels	
RTC		Programmable Alarm A, 2 external tamper check	
CRC		Three CRCs with polynomial options	
Conditions	Operating Temperature	Ambient Temperature:-40℃ to +85℃ Conjunction Temperature: -40℃ to +105℃	
	Operating Voltage	2.5V to 5.5V	
Package Information		LQFP64	LQFP48

1. TIM1
2. TIM2/TIM3/TIM4
3. TIM6

3 Pinouts and Pin Description

3.1 BS32F103xBT6 pin package and function definition

Figure 3.1 BS32F103CBT6 package pins

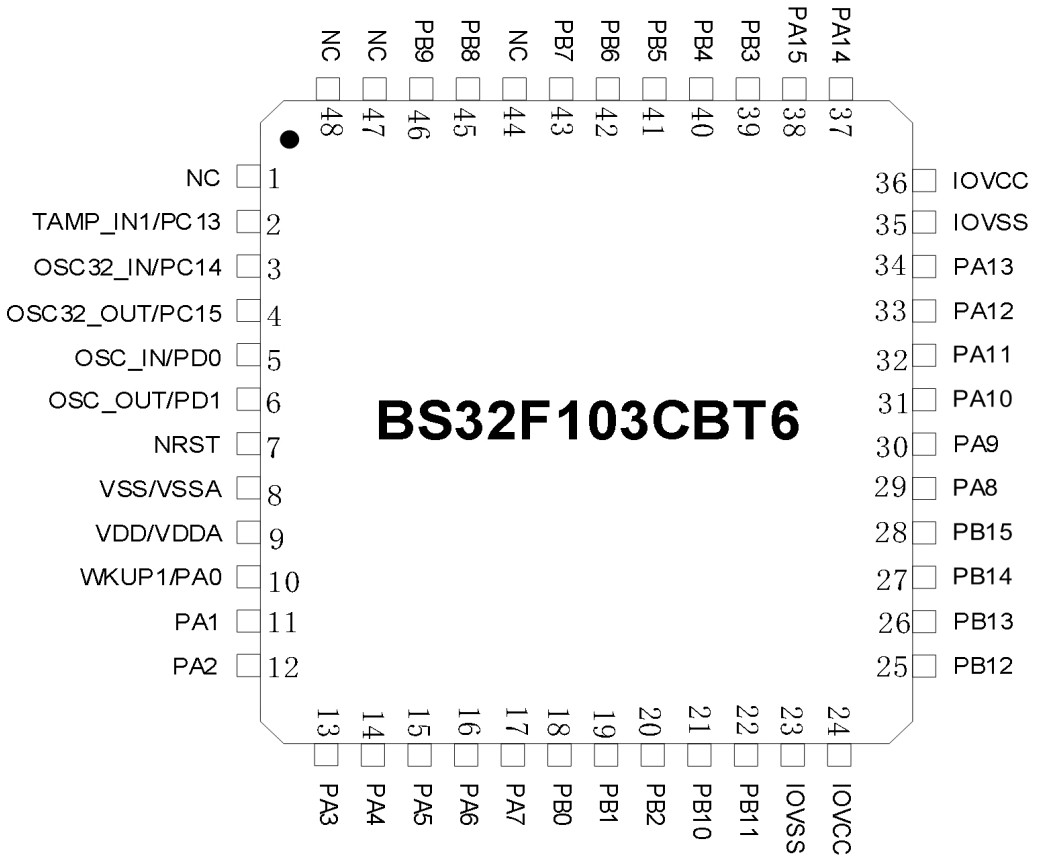


Figure 3.2 BS32F103RBT6 package pins

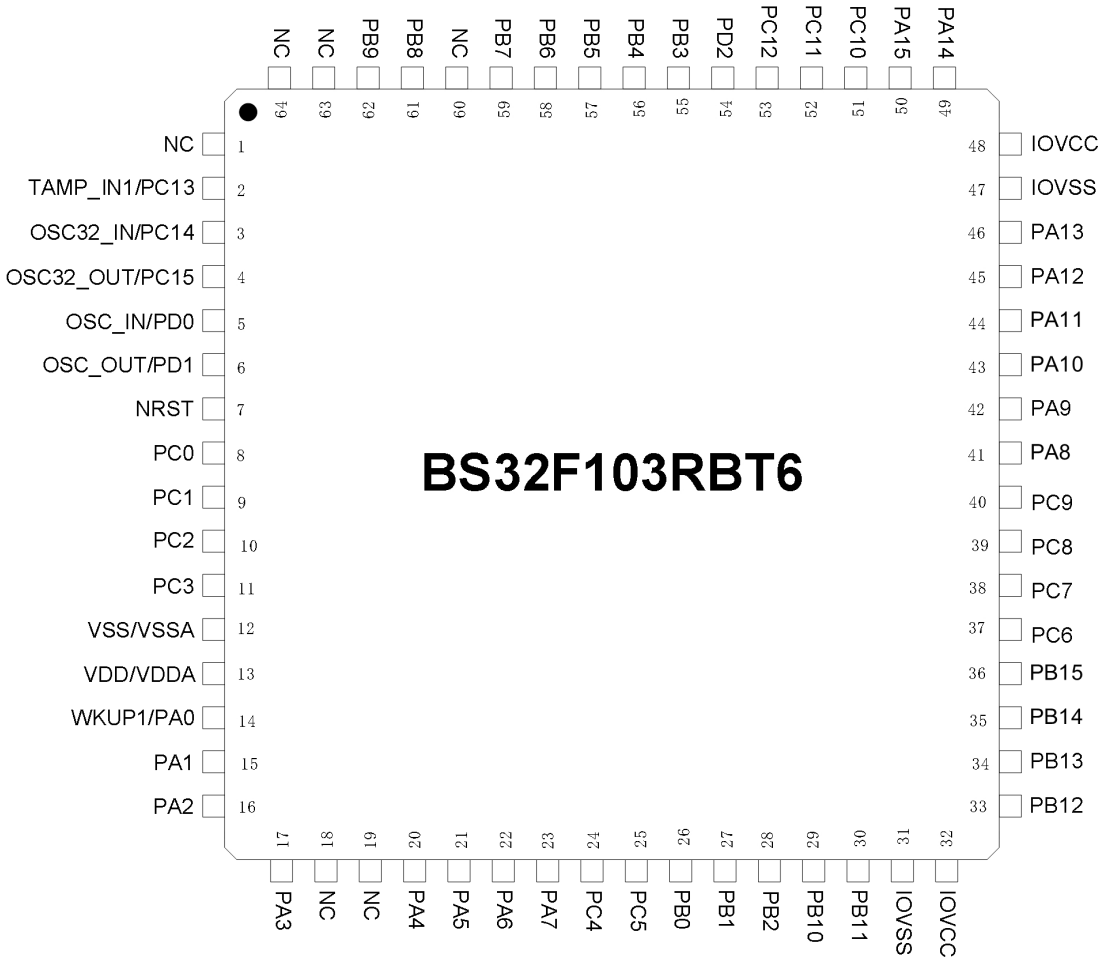


Table 3.1 BS32F103xBT6 pin definitions

Pin number		Pin name	Pin type	Note	Pin functions		
LQFP64	LQFP48				Default functions(After reset)	Alternate functions	Additional functions
1	1	-	-	-	-	-	-
2	2	PC13	I/O	-	PC13	-	RTC_OUT1/ TAMP_IN1/WKUP2
3	3	PC14	I/O	-	PC14	-	OSC32_IN
4	4	PC15	I/O	-	PC15	OSC32_EN	OSC32_OUT
5	5	PD0	I/O	-	PD0	-	OSC_IN
6	6	PD1	I/O	-	PD1	OSC_EN	OSC_OUT
7	7	NRST	I	-	NRST	-	-
8	-	PC0	I/O	-	PC0	-	ADC1/2_IN10
9	-	PC1	I/O	-	PC1	-	ADC1/2_IN11
10	-	PC2	I/O	-	PC2	-	ADC1/2_IN12
11	-	PC3	I/O	-	PC3	-	ADC1/2_IN13
12	8	VSSA	S	-	VSS/VSSA	-	-
13	9	VDDA	S	-	VDD/VDDA	-	-
14	10	PA0	I/O	-	PA0	UART2_CTS/TIM2_ETR/ TIM2_CH1	ADC1/2_IN0/WKUP1/ TAMP_IN2
15	11	PA1	I/O	-	PA1	UART2_RTS_DE/TIM2_CH2	ADC1/2_IN1
16	12	PA2	I/O	-	PA2	UART2_TX/TIM2_CH3	ADC1/2_IN2/WKUP4
17	13	PA3	I/O	-	PA3	UART2_RX/TIM2_CH4	ADC1/2_IN3
18	-	-		-	-	-	-
19	-	-		-	-	-	-

Table 3.1 BS32F103xBT6 pin definitions (continued)

Pin number		Pin name	Pin type	Note	Pin functions		
LQFP64	LQFP48				Default functions(After reset)	Alternate functions	Additional functions
20	14	PA4	I/O	-	PA4	SPI1_NSS	ADC1/2_IN4
21	15	PA5	I/O	-	PA5	SPI1_SCK/TIM4_ETR	ADC1/2_IN5
22	16	PA6	I/O	-	PA6	SPI1_MISO/TIM1_BKIN/ TIM3_CH1	ADC1/2_IN6
23	17	PA7	I/O	-	PA7	SPI1_MOSI/TIM1_CH1N/ TIM3_CH2	ADC1/2_IN7
24	-	PC4	I/O	-	PC4	-	ADC1/2_IN14
25	-	PC5	I/O	-	PC5	-	ADC1/2_IN15
26	18	PB0	I/O	-	PB0	TIM1_CH2N/TIM3_CH3	ADC1/2_IN8
27	19	PB1	I/O	-	PB1	TIM1_CH3N/TIM3_CH4	ADC1/2_IN9
28	20	PB2	I/O	-	-	-	-
29	21	PB10	I/O	-	PB10	I2C2_SCL/UART3_TX/ TIM2_CH3	
30	22	PB11	I/O	-	PB11	I2C2_SDA/UART3_RX/ TIM2_CH4	
31	23	IOVSS	S	-	IOVSS	-	-
32	24	IOVCC	S	-	IOVCC	-	-
33	25	PB12	I/O	-	PB12	SPI2_NSS/TIM1_BKIN	-
34	26	PB13	I/O	-	PB13	SPI2_SCK/UART3_CTS/ TIM1_CH1N	-
35	27	PB14	I/O	-	PB14	SPI2_MISO/UART3_CTS/ TIM1_CH2N	-
36	28	PB15	I/O	-	PB15	SPI2_MOSI/UART3_RTS_D/ TIM1_CH3N	-
37	-	PC6	I/O	-	PC6	TIM3_CH1	-
38	-	PC7	I/O	-	PC7	TIM3_CH2	-
39	-	PC8	I/O	-	PC8	TIM3_CH3	-

Table 3.1 BS32F103xBT6 pin definitions (continued)

Pin number		Pin name	Pin type	Note	Pin functions		
LQFP64	LQFP48				Default functions(After reset)	Alternate functions	Additional functions
40	-	PC9	I/O	-	PC9	TIM3_CH4	-
41	29	PA8	I/O	-	PA8	TIM1_CH1/MCO	-
42	30	PA9	I/O	-	PA9	UART1_TX/TIM1_CH2	-
43	31	PA10	I/O	-	PA10	UART1_RX/TIM1_CH3	-
44	32	PA11	I/O	-	PA11	UART1_CTS/TIM1_CH4/ CANRX	-
45	33	PA12	I/O	-	PA12	UART1_RTS_DE/TIM1_ETR/ CANTX	-
46	34	PA13	I/O	-	SWDIO	-	-
47	35	IOVSS	S	-	IOVSS	-	-
48	36	IOVCC	S	-	IOVCC	-	-
49	37	PA14	I/O	-	SWCLK	-	-
50	38	PA15	I/O	-	PA15	SPI1_NSS/TIM2_CH1/ TIM2_ETR	-
51	-	PC10	I/O	-	PC10	UART3_TX	-
52	-	PC11	I/O	-	PC11	UART3_RX	-
53	-	PC12	I/O	-	PC12	-	-
54	-	PD2	I/O	-	PD2	TIM3_ETR	-
55	39	PB3	I/O	-	PB3	SPI1_SCK/TIM2_CH2	-
56	40	PB4	I/O	-	PB4	SPI1_MISO/TIM3_CH1	-
57	41	PB5	I/O	-	PB5	SPI1_MOSI/TIM3_CH2	WKUP6
58	42	PB6	I/O	-	PB6	I2C1_SCL/TIM4_CH4/ UART1_TX	-
59	43	PB7	I/O	-	PB7	I2C1_SDA/TIM4_CH2/ UART1_RX	-
60	44	-	-	-	-	-	-

Table 3.1 BS32F103xBT6 pin definitions (continued)

Pin number		Pin name	Pin type	Note	Pin functions		
LQFP64	LQFP48				Default functions(After reset)	Alternate functions	Additional functions
61	45	PB8	I/O	-	PB8	I2C1_SCL/TIM4_CH3/ CANRX	-
62	46	PB9	I/O	-	PB9	I2C1_SDA/TIM4_CH4/ CANTX	-
63	47	-	-	-	-	-	-
64	48	-	-	-	-	-	-

Table 3.2 Port A alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	Configurations (Priority from high to low)			
PA0	-	UART2_CTS	TIM2_ETR	TIM2_CH1	ADC1/2_IN0	WKUP1	TAMP_IN2	-
PA1	-	UART2_RTS _DE	-	TIM2_CH2	ADC1/2_IN1	-	-	-
PA2	-	UART2_TX	-	TIM2_CH3	ADC1/2_IN2	WKUP4	-	-
PA3	-	UART2_RX	-	TIM2_CH4	ADC1/2_IN3	-	-	-
PA4	SPI1_NSS	-	-	-	ADC1/2_IN4	-	-	-
PA5	SPI1_SCK	TIM4_ETR	-	-	ADC1/2_IN5	-	-	-
PA6	SPI1_MISO	TIM1_BKIN	-	TIM3_CH1	ADC1/2_IN6	-	-	-
PA7	SPI1_MOSI	TIM1_CH1N	-	TIM3_CH2	ADC1/2_IN7	-	-	-
PA8	-	TIM1_CH1	MCO	-	-	-	-	-
PA9	UART1_TX	TIM1_CH2	-	-	-	-	-	-
PA10	UART1_RX	TIM1_CH3	-	-	-	-	-	-
PA11	UART1_CTS	TIM1_CH4	CANRX	-	-	-	-	-
PA12	UART1_RTS _DE	TIM1_ETR	CANTX	-	-	-	-	-
PA13	SWDIO	-	-	-	-	-	-	-
PA14	SWCLK	-	-	-	-	-	-	-
PA15	-	SPI1_NSS	TIM2_CH1	TIM2_ETR	-	-	-	-

1. For PA4, configure the third part of its functions, and its priority can be set in RTC module.

Table 3.3 Port B alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	Configurations (Priority from high to low)			
PB0	-	TIM1_CH2N	-	TIM3_CH3	ADC1/2_IN8	-	-	-
PB1	-	TIM1_CH3N	-	TIM3_CH4	ADC1/2_IN9	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	-	SPI1_SCK	TIM2_CH2	-	-	-	-	-
PB4	-	SPI1_MISO	-	TIM3_CH1	-	-	-	-
PB5	-	SPI1_MOSI	-	TIM3_CH2	-	WKUP6	-	-
PB6	I2C1_SCL	TIM4_CH1	UART1_TX	-	-	-	-	-
PB7	I2C1_SDA	TIM4_CH2	UART1_RX	-	-	-	-	-
PB8	I2C1_SCL	TIM4_CH3	CANRX	-	-	-	-	-
PB9	I2C1_SDA	TIM4_CH4	CANTX	-	-	-		-
PB10	I2C2_SCL	UART3_TX	TIM2_CH3	-	-	-	-	-
PB11	I2C2_SDA	UART3_RX	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS	-	-	TIM1_BKIN	-	-	-	-
PB13	SPI2_SCK	-	UART3_CTS	TIM1_CH1N	-	-	-	-
PB14	SPI2_MISO	-	UART3_RTS_DE	TIM1_CH2N	-	-	-	-
PB15	SPI2_MOSI	-	-	TIM1_CH3N	-	-	-	-

Table 3.4 Port C alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	Configurations (Priority from high to low)			
PC0	-	-	-	-	ADC1/2_IN10	-	-	-
PC1	-	-	-	-	ADC1/2_IN11	-	-	-
PC2	-	-	-	-	ADC1/2_IN12	-	-	-
PC3	-	-	-	-	ADC1/2_IN13	-	-	-
PC4	-	-	-	-	ADC1/2_IN14	-	-	-
PC5	-	-	-	-	ADC1/2_IN15	-	-	-
PC6	-	TIM3_CH1	-	-	-	_	-	-
PC7	-	TIM3_CH2	-	-	-	_	-	-
PC8	-	TIM3_CH3	-	-	-	_	-	-
PC9	-	TIM3_CH4	-	-	-	_	-	-
PC10	-	UART3_TX	-	-	-	_	-	-
PC11	-	UART3_RX	-	-	-	_	-	-
PC12	-	-	-	-	-	_	-	-
PC13	_	-	-	-	-	WKUP2	TAMP_IN1	RTC_OUT1
PC14	_	-	-	-	-	OSC32_IN	OSC32_IN	-
PC15	OSC32_EN	-	-	-	-	OSC32_OUT	-	-

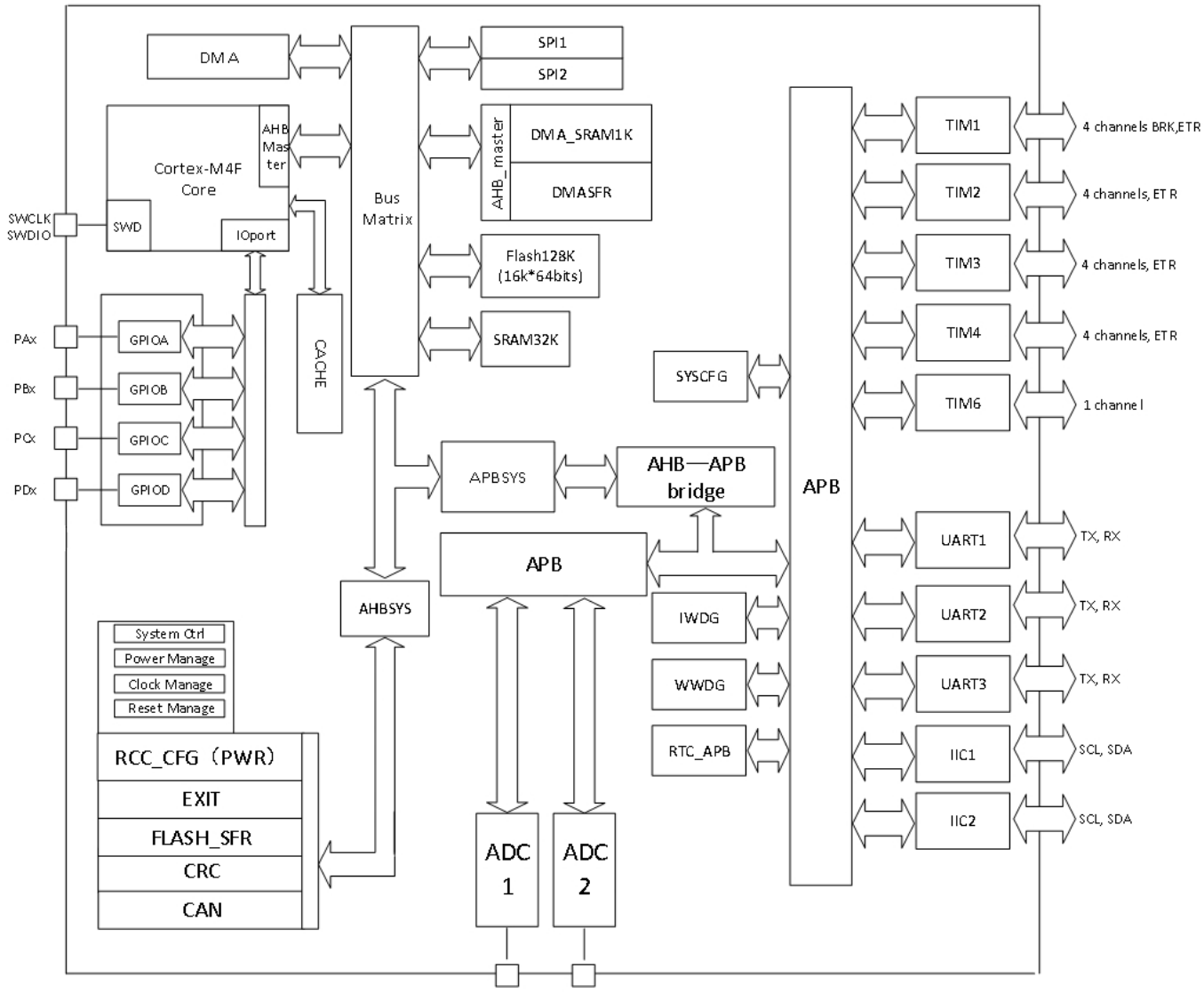
Table 3.5 Port D alternate and additional functions

GPIO	AF0	AF1	AF2	AF3	Configurations (Priority from high to low)			
PD0	-	-	-	-	-	OSC_IN	OSC_IN	-
PD1	OSC_EN	-	-	-	-	OSC_OUT	-	-
PD2	TIM3_ETR	-	-	-	-	-	-	-

4 System Block Diagram

BS32F103xBT6 microcontrollers family are equipped with many peripherals, which have AHB and APB buses. Different peripherals are on the different buses according to functional requirements to improve the efficiency of the system running. Figure 4.1 shows the system block diagram.

Figure 4.1 BS32F103xBT6 block diagram



5 Memory Mapping

System allocates different address space to different peripherals, refer to Reference Manual. *Table 5.1 List of address mapping* shows a table of address mapping.

Table 5.1 List of address mapping

Module	Base address	End address
Reserved	0x5000_1000	0x5000_17FF
GPIOD	0x5000_0C00	0x5000_0FFF
GPIOC	0x5000_0800	0x5000_0BFF
GPIOB	0x5000_0400	0x5000_07FF
GPIOA	0x5000_0000	0x5000_03FF
DMASFR	0x4003_0400	0x4003_07FF
DMA_SRAM	0x4003_0000	0x4003_03FF
CAN	0x4002_4000	0x4002_43FF
CRC	0x4002_3000	0x4002_33FF
FLASH_SFR	0x4002_2000	0x4002_23FF
EXTI	0x4002_1800	0x4002_1BFF
RCC	0x4002_1000	0x4002_13FF
SPI2	0x4002_A400	0x4002_A7FF
SPI1	0x4002_A000	0x4002_A3FF
System Setting	0x4001_4800	0x4001_4BFF
	0x4001_4400	0x4001_47FF
	0x4001_4000	0x4001_43FF
UART1	0x4001_3800	0x4001_3BFF
TIM2	0x4001_3000	0x4001_33FF
TIM1	0x4001_2C00	0x4001_2FFF
ADC1	0x4001_2400	0x4001_27FF
ADC2	0x4001_0000	0x4001_03FF
I2C2	0x4000_5800	0x4000_5BFF
I2C1	0x4000_5400	0x4000_57FF
UART2	0x4000_4400	0x4000_47FF
UART3	0x4000_3800	0x4000_3BFF
IWDG	0x4000_3000	0x4000_33FF
WWDG	0x4000_2C00	0x4000_2FFF
RTC	0x4000_2800	0x4000_2BFF
TIM4	0x4000_2000	0x4000_23FF
TIM6	0x4000_1000	0x4000_13FF
TIM3	0x4000_0400	0x4000_07FF
AHB2APB	0x4000_0000	0x4001_63FF
SRAM	0x2000_0000	0x2000_7FFF
System Information Block	0x0002_0200	0x0002_03FF
Option Byte Block	0x0002_0000	0x0002_01FF

1. User is not allowed to configure the system settings.

6 Functional Overview

6.1 ARM® Cortex® -M4F Core

The ARM®-Cortex®-M4F core is a mainstream 32-bit Cortex processor with a Von-Neumann architecture that adds floating point, DSP, and parallel computing for enhanced computing power and RISC for superior performance with a lean instruction set. It has higher code density and more comprehensive optimization than other 8-bit and 16-bit microcontrollers, and is highly compatible with other Cortex-M for digital signal control markets that require an easy-to-use mix of control and signal processing functions: include solutions for motor control, automotive, power management, embedded audio, and other emerging categories.

The ARM® Cortex® -M4F Core is widely used in design of embedded products, with integrated memory protection Unit (MPU) and ultra-low power consumption, supporting KEIL&IAR mainstream development tools, which is easy for developers to program, implement and debug the product functions.

6.2 Flash memory

The BS32F103xBT6 devices offer a 128Kbytes of Flash memory for storing code and data, without ECC function.

The address ranges from 0x0000_0000 to 0x0001_FFFF.

Flash memory supports IAP Boot upgrade.

With the configuration option byte, you can flexibly configure read/write protection:

- Readout protection (RDP) to protect the whole memory. Two levels are available:
  - Level 0: no readout protection
  - Level 1: enable readout protection
- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.

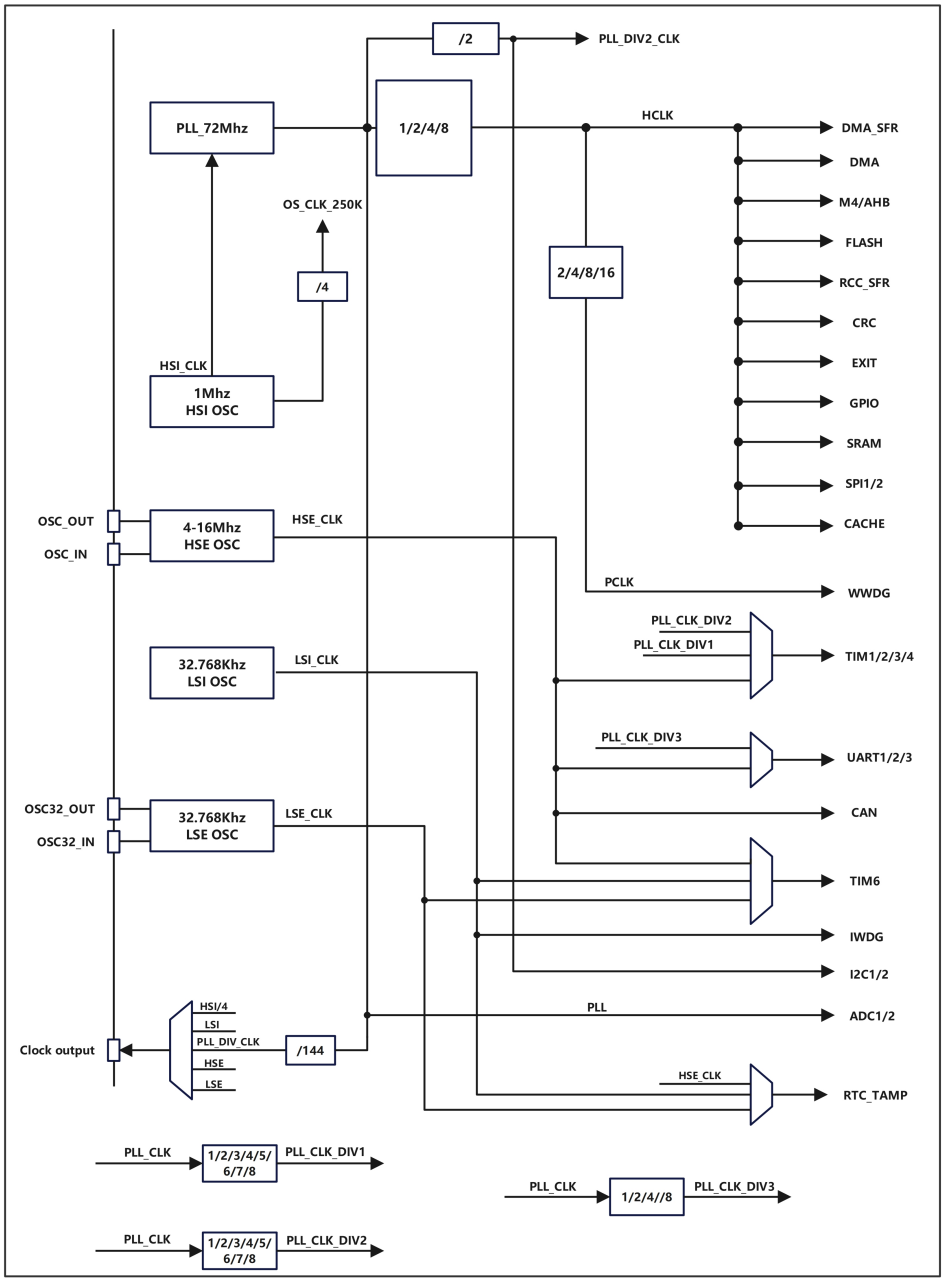
6.3 SRAM Memory

The BS32F103xBT6 devices offer 32Kbytes of SRAM. The address ranges form 0x2000_0000 to 0x2000_7FFF.

6.4 Clock

System clock source is 1MHz internal RC oscillator, which is multiplexed to generate PLL, supplying clock to the Core and the peripherals. It also manages clock gating and multi-level prescalers for low-power mode and ensures clock robustness. The clock source of IWDG is always LSI.

Figure 6.1 BS32F103xBT6 system clock tree



6.5 Power management

6.5.1 Power supply schemes

The BS32F103xBT6 devices require a operating voltage (V_{DD}) of 2..5V to 5.5V, power supply scheme:

- V_{DD}=2..5V to 5.5V

6.5.2 Power supply monitor

The device has an integrated power-on/power-down reset (POR/PDR) active in all power modes with BOR threshold value configurable. The integrated LVDT, threshold is also configurable.

6.5.3 Low-power Modes

By default, the microcontrollers is in Run mode after system or power reset. It is up to the user to select one of the low-power modes as follows:

- Sleep Mode
- Deepsleep Mode
- Shutdown Mode

Table 6.1 Low-power mode and wake-up sources

Low-power mode and wake-up sources	**Sleep Mode:** - All operating peripherals interrupt - IWDG reset - BOR reset - NRST external reset

	Deepsleep: - Any interrupt on EXTI line - TIM6 interrupt - RTC/TAMP interrupt - I2C interrupt - CAN interrupt - UART interrupt - LVDT interrupt - IWDG reset - BOR reset - NRST external reset
Low-power mode and wake-up sources	**Shutdown:** - WKUP pin - RTC/TAMP interrupt - NRST external reset - BOR reset

6.6 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a master bus system peripheral,which uses a single AHB master bus architecture.Without CPU intervention,DMA can transfer data between peripherals and memory or between memory and memory.

The DMA has 32 independent configurable channels,and each channel corresponds to a fixed peripheral request..

- Each DMA channel with two-level priority configurable
- Support DMA data transfers as follows:
  - — Memory-to-memory
  - — Memory-to-peripheral
  - — Peripheral-to-memory
- Support three DMA data transfer size: word, half-world, byte.
- The number of data to be transferred in a single DMA cycle is from 1 to 1024, the unit depends on the data transfer size.
- An interrupt is generated when any channel completes the data transfer or occurs bus error, each channel has an independent interrupt enable, transfer finish flag and error interrupt flag.

6.7 Cyclic redundancy check calculation unit (CRC)

CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time.

- Three CRC polynomial options:
  - CRC-32: polynomial 32'h04C11DB7 (by default)
  - CRC-16: polynomial 16'h1021
  - CRC-8: polynomial 8'h07
- Handles 8-, 16-, 32-bit data size:
  - 4 AHB clock cycles for 32-bit
  - 2 AHB clock cycles for 16-bit
  - 1 AHB clock cycles for 8-bit
- Initial value, XOR value configurable

6.8 General-purpose inputs/outputs (GPIO)

Each of the BS32F103xBT6 GPIO pins can be configured by software as output/input or as peripheral alternate function (AF). All GPIO pins can be mapped to external interrupts. Most of the GPIO pins are shared with special digital or analog functions.

- Output states: push-pull/open drain output with pull-up/down resistor
- Input states: floating input, pull-up/down resistor, analog input
- Each of the GPIO pins with speed options (2M/10M/50M)
- Fast switching, able to switch every two clock cycles
- With internal 40K pull-up/down resistor
- IO sink current is 20mA@3.3V
- IO source cuent is 8mA@3.3V
- All I/O overcurrent is 100mA

6.9 Interrupts

The device flexibly manages events causing interrupts of linear program execution, called interrupts. The Cortex-M4F processor core, nested vectored interrupt controller (NVIC) and extended interrupt/event controller (EXTI) are used to handle the interrupts. Interrupts result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

6.9.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the M4F core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupt-related events, and Cortex-M4F interrupts. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- Three fixed maximum priorities and 16 programmable priorities
- Handling of a Non-maskable interrupt(NMI)
- Handling of 32 maskable interrupt lines
- Handling of 37 shieldable interrupt lines
- Later-arriving higher-priority interrupt processed first
- Support for tail-chaining
- Interrupt vector retrieval by hardware

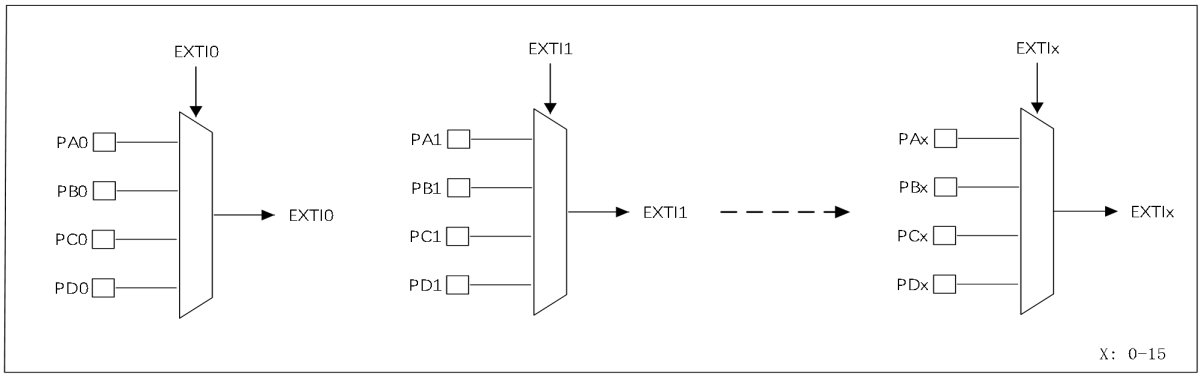
6.9.2 External interrupt controller (EXIT)

The extended interrupt controller adds flexibility in handling physical line events and

allows processor wakeup from Low-power mode.

- System wakeup upon event on any input
- Selectable active trigger edge (rising, falling, both edges)
- Detection of trigger edge wakeup system
- Independent rising and falling edge interrupt pending status bits
- Independent interrupt masking, used for conditioning the CPU wakeup
- Interrupts (EXIT Lines 0-15) with GPIO interrupt source selectable

Figure 6.2 EXTI GPIO multiplexer



1. Some of the pins of ports 0-15 are not complete,and the ports that exist are configured according to the above rules.
2. The output of EXTI multiplexer can be used as the output signal of EXTI.

6.10 Analog-to-digital converter (ADC)

BS32F103xBT6 devices embedded a successive approximation ADC with 8-bit (its data resolution is right-aligned) and12-bit selectable. For package LQFP64 the ADC has up to 18 channels (16 external inputs, 1 internal reference voltage and 1 internal temperature sensor). For LQFP48, the ADC has up to 12 channels (10 external inputs + 1 from internal reference voltage + 1 internal temperature sensor).

ADC can be performed in single mode and continuous multi-channel DMA mode with the sampling time and conversion rate configurable.

ADC generates an interrupt upon the conversion finishes. The event trigger indicates that the start of the conversion is triggered by software or hardware.

ADC supports wakeup from Sleep Mode.

Way to start the conversion:

- Triggered by software
- Triggered by internal event (Timer1 event) or hardware

Table 6.2 BS32F103xBT6 Timer Feature comparison table

ADC Feature	ADC1	ADC2
Supports 1M conversion rate	√	√
Supports multi-channel conversion	√	√
Support timer trigger	√	√
Wake up from Sleeping mode is supported	√	√

6.11 Timers and watchdogs

The BS32F103xBT6 includes an advanced-control timer (TIM1), three general-purpose timers (TIM2, TIM3, TIM4), a basic timer, two watchdog timers and a SysTick timer. Table 6.3 compares features of the advanced-control, general-purpose and basic timers.

Table 6.3 BS32F103xBT6 Timer Comparison

Timer Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request Generation	Capture /compare channels	Dead time complementary output channels
Advanced	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	3
General	TIM2	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	0
General	TIM3	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	0
General	TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	0
Basic	TIM 6	20-bit	Up	-	-	-	

6.11.1 Advanced-control timer (TIM1)

The advanced-control timer features include 16-bit up, down, up/down auto-reload counter, 16-bit programmable prescaler allowing dividing the counter clock frequency by any integer between 1 to 65536.

Up to 6 independent channels for:

- Input capture (but channel 5 and 6)
- Output compare
- PWM generation (edge- and center-aligned modes)
- One-pulse mode output

The advanced-control timer (TIM1) offers complementary outputs with programmable dead-time and one break inputs to put the timer's output signals in a reset state or a known state.

TIM1 provides a synchronization circuit to control the timer with external signals and to interconnect several timers together. It also has a repetition counter that updates the timer registers only after a given number of cycles of the counter.

Interrupt/DMA request generation upon the following events:

- Update: counter overflow, counter initialization (by software or internal/external trigger)
- Trigger event: (counter start, stop, initialization or count by internal/external trigger)
- Input capture
- Output campare
- Break input (only interrupt requests can be generated,but no DMA request)

The advanced-control timer can be used to triggering ADC, and supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes.

Trigger input can serve as an external clock or cycle-by-cycle current management.

6.11.2 General-purpose timer (TIMx,x=2,3,4)

TIMx timer features include:

16-bit up, down, up/down auto-reload counter, 16-bit programmable prescaler used to divide the counter clock frequency by any integer between 1 to 65536,Up to 4 independent channels for:

- Input capture
- Output compare
- PWM generation (edge- and center-aligned modes)
- one-pulse mode output

Synchronization circuit to control the timer with external signals and to interconnect several timers.Interrupt/DMA generation on the following events:

- Update: counter overflow, counter initialization (by software or internal/external trigger)
- Trigger event: (counter start, stop, initialization or count by internal/external trigger)

- Input capture
- Output compare

Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes.

Trigger input for external clock or cycle-by-cycle current management

6.11.3 Basic timer (TIM6)

The basic timer (TIM6) consists of a 20-bit up auto-reload counter, the clock source includes LSI, LSE or HSE. Refer to *Figure 6.1 BS32F103xBT6 System clock tree* for details.

System can be woken up in Deepsleep Mode.

6.11.4 Independent watchdog (IWDG)

The independent watchdog has a 20-bit up counter with a prescaler factor configurable options. The maximum counting value is configurable. The maximum configurable time is 32s, and the clock source is LSI.

IWDG features register write-protection, which enables and disables WDT by configuring byte, and window mode is selectable.

Reset generates when:

- Generate a reset when the counter value is greater than or equal to the configured maximum value；

6.11.5 Window watchdog (WWDG)

The window watchdog (WWDG) is based on a 6-bit up counter. It is clocked by PCLK, which frequency is divided with a prescaler factor of 4096 before another frequency division. The prescaler factor is configurable with options (1/2/4/8/16/32/64/128).

- Feeding dog operation: write a value to a certain register, this value is loaded into counter.
- Window mode: selectable (No enable control, by default, the window value is 0, which indicates the window is invalid)
- Reset conditions (When WDG enable is valid)

  - Reset when the counter value is greater than or equal to the maximum value of the configuration

  -Reset when the counter value is less than the window value
- Interrupt: triggered when the up counter is equal to the maximum value minus 1 (if

interrupt enable is configured), which is used to remind system of a coming reset.

6.11.6 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

It has the following Features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- HCLK as Clock source

6.12 Real-time clock (RTC)

The device embeds a RTC and five backup registers. The supply voltage of the RTC is V_{DD}. It has a write protection feature.

Features of the RTC:

- Calendar with subsecond (maximum value configurable), seconds, minutes, hours (24 format)
- Calendar can be initialized,RTC domain can be reset by writing registers
- A Programmable alarm A (any clock within the counter range)
- Outputs of the alarm A and tamper events to pins
- Outputs of a 1Hz clock, LSI and LSE to pins
- RTC can wake up system from low-power mode
- Supports alarm interrupt, second interrupt, day interrupt and tamper interrupt

6.13 Tamper and backup register (TAMP)

Features of the TAMP:

- Five 32-bit backup registers
- Two external tamper detection pins TAMP1/2
- Any tamper detection can erase the backup registers (erase enable configurable)

6.14 Inter-integrated circuit interface (I2C)

The device embeds two I2C peripherals. Refer to *Table 6.4 12C features* for details.

Features of the I2C:

- Master and slave mode
- Standard mode (up to 100kHz)
- Fast mode (up to 400kHz)
- Super fast mode (up to 1MHz)
- 7-bit addressable mode
- General call
- Two 7-bit slave addresses (1 with configurable mask)
- Parameters of Master timing configurable
- Optional clock stretching
- Software Reset (Register enable is shut down, Internal states machines and the related timing are reset)
- DMA transmission support
- Wakeup from Deepsleep mode on address match

Table 6.4 I2C features

I2C features	I2C1	I2C2
100K,400K,1M communication rate support	√	√
7-bit address	√	√
Wakeup from Deepsleep Mode	√	√

6.15 Serial peripheral Interface (SPI)

The device embeds two SPIs, supporting half-duplex and full-duplex communications. SPI can be configured as master or slave mode. In master mode, clock and chip select signals are generated and output by SPI module, while clock and chip select signals are from external inputs in slave mode. The communication speed is up to 16M in master mode and 8M in slave mode. The data size is configurable from 4-bit to 16-bit to 32-bit.

SPI features programmable clock polarity and phase, the sequence of high bit and low bit to be set, two 32-bit receive/transmit buffer supporting DMA capability, dedicated transmission and reception flags with interrupt capability, overflow flags with interrupt capability in case of master mode fault, SPI bus busy status flag and Hardware CRC support.

6.16 Universal asynchronous receiver transmitter (UART)

The device embeds three identical UART modules with independently enabled double buffer receiver/transmitter. It supports half-duplex, full-duplex serial port communications and hardware parity generation and checks. It uses programmable data word length (8 or 9 bits) and configurable 1 or 2 stop bits.

It supports auto baud rate feature and oversampling by 16, with programmable baud rate (15-bit analog-digital divider), adapt common baud rate(2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400).

UART supports continuous communications using DMA(Direct memory access). Received/transmitted bytes are buffered in reserved SRAM using DMA.

UART features swappable RX/TX pin configuration whose active level can inverse. Programmable data order with MSB-first or LSB (default setting)-first shifting, separate enable bits for receiver/transmitter, separate signal polarity control for transmission and reception, hardware flow control for modem and RS-485 transceiver, communication control/error detection flags, interrupt sources with flags and multiprocessor communications (wakeup from Mute mode by idle line detection or address mark detection if addresses do not match and the device enters mute mode).

Parity control:

- Transmit parity bit
- Checks parity of received data byte

Table 6.5 UART features

UART features	UART1/UART2/UART3
Hardware flow control for MODEM	√
Continuous communication using DMA	√
Multiprocessor communication	√
Wakeup from Deepsleep mode	√
Idle interrupt	√
Auto baud rate detection	√
RS485 driver enable signal	√

6.17 Controller LAN interface (CAN)

CAN interface compatibility specifications 2.0A and 2.0B (active) (sending and receiving of standard and extended frame information at bit rates up to 1Mbit/ s.It can receive and send standard frames with 11-bit identifiers and also has the following features:

- Lossless arbitration
- High bus utilization, allowing any cell to start sending packets as long as the bus is idle.
- According to the PACKET ID, the user decides to accept or block a packet.
- Mechanism for fault handling and fault checking.
- A user automatically resends a message after it is damaged.
- A node functions to exit the bus automatically if an error is critical.
- Supports a low-power Deepsleep wake up function.
- Lent has single/dual acceptance filters with shielding and code registers in both standard and extended formats.
- A programmable error limiting alarm.
- A passive fault interrupt, arbitration lost-interrupt, and bus fault interrupt.
- Lent supports normal mode, silent mode, and loop self-test mode.
- Arbitrate loses interrupts and loses the detailed bit position.
- Sending buffer FIFO and receiving buffer FIFO.
- Supports DMA to send and receive messages.

6.18 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

7 Electrical Characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions on the production line through tests performed on 100% of the products at ambient temperatures TA = 25℃ and TA = TAmax (TAmax matches the selected temperature range).

Data obtained through comprehensive evaluation, design simulation and / or process characteristics are described in the notes below each table and will not be tested on the production line ; on the basis of comprehensive evaluation, the minimum and maximum values are obtained by the standard distribution of three times the average value of the sample test.

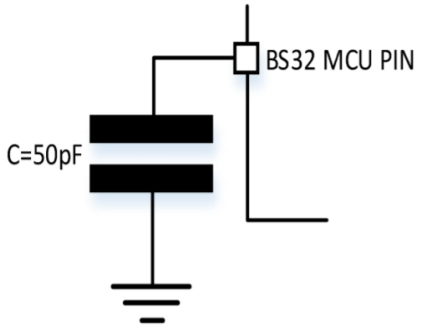
7.1.2 Typical values

Unless otherwise specified, typical data are based on TA = 25℃ and VDD = 3.3V. These data are used for design guidance only and not for testing.

7.1.3 load capacitance

The load conditions for measuring the pin parameters are shown in Figure 7.1.

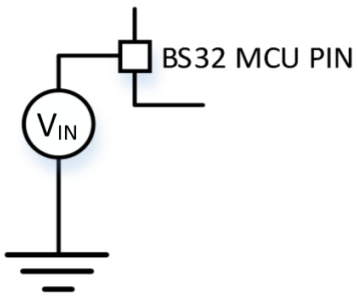
Figure.7.1 Load conditions of pins



7.1.4 Pin input voltage

The measurement of the input voltage on the pin is shown in Figure 7.2.

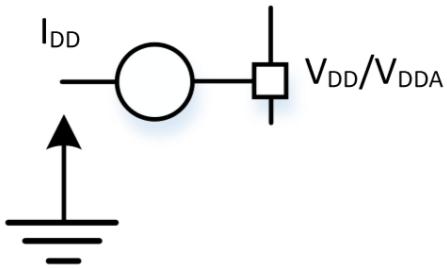
Figure 7.2 Pin input voltage



7.1.5 Current consumption measurement

The I_{DD} parameter in Figure 7.3 represents the total current consumption of the MCU powered by V_{DD} / V_{DDA}.

Figure 7.3 Current consumption measurement



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 7.1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}/V_{DDA}	External supply voltage	V_{SSA}-0.3	V_{SSA}+5.5	V
V_{IN}(2)	Input voltage on pin	V_{SS}-0.3	5.5	V
I_{VDD}(PIN)	Current (Source current) entering the V_{DD} / V_{DDA} power supply pin	-	120	mA
I_{VSS}(PIN)	The current flowing out of the V_{SS} / V_{SSDA} grounding pin (Sink current)	-	120	mA

I_{IO}	Output current on any I / O pin	-	50	mA
	Output pull current on any I / O pin	-	50	mA
$\Sigma I_{IO(PIN)}$	Total output current on all I / O pins	-	100	mA
	Total output pull current on all I / O pins	-	100	mA
T_A	operating temperature range	-40	85	°C
T_{STG}	Storage temperature range	-45	125	°C
T_J	Maximum junction temperature	-	125	°C

1.The main power(V_{DD}/V_{DDA}) and ground(V_{SS}/V_{SSA}) pins must always be connected to an external power supply within the allowable range.

2.Not allowed V_{IN} greater than V_{IOVCC}

7.3 General working conditions

Table 7.2 General working conditions

Sign	Parameters	Min	MAX	Unit
f_{HCLK}	AHB clock frequency	0	72	MHZ
f_{PCLK}	APB clock frequency	0	36	MHZ
V_{DD}/V_{DDA}	supply voltage	2.5	5.5	V
V_{IOVCC}(1)	I/O supply voltage	2.5	5.5	V
V_{IN}	IO input voltage	0	V_{IOVCC}	V
T_A	working temperature	-40	85	℃
T_J	Junction Temperature	-40	105	℃

1.V_{IOVCC} is equal to the input V_{DDA}.

7.4 GPIO characteristics

Unless otherwise stated, the parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conditions summarized in the general operating conditions. All I/Os meet CMOS and TTL standards.

Table 7.3 GPIO Characteristics

Sign	Parameters	Min	Typ	Max	Unit
V_{OH}	I/O output high level voltage	90	-	-	%V_{IOVCC}(1)
V_{OL}	I/O output low level voltage	-	-	10	%V_{IOVCC}
V_{IH}	I/O output high level voltage	70	-	-	%V_{IOVCC}
V_{IL}	I/O output low level voltage	-	-	30	%V_{IOVCC}
V_{hys}(2)	Standard I/O Schmitt trigger voltage hysteresis	10	-	-	%V_{IOVCC}

R_{PU}	Pull-up equivalent resistance	-	40	-	KΩ
R_{PD}	Equivalent pull-down resistance	-	40	-	KΩ

1. The hysteresis voltage of Schmidt trigger switch level. Guaranteed by the design, not tested in production.
2. The pull-up and pull-down resistors are designed as a real resistor in series with a switchable PMOS / NMOS implementation. The resistance ratio of PMOS / NMOS switch is very small.

7.5 Energy consumption characteristics

Table 7.4 Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}/I_{DDA}	Supply current (run mode)	V_{DD}=3.3V, T_A=25°C	-	20.75	-	mA
	Supply current (sleep mode)	V_{DD}=3.3V, T_A=25°C	-	5.9	-	mA
	Supply current (deepsleep mode)	V_{DD}=3.3V, T_A=25°C	-	8.7	-	uA
	Supply current (shutdown mode)	V_{DD}=3.3V, T_A=25°C	-	2.3	-	uA

7.6 Internal reset and power manager characteristics

The following parameters are obtained from the ambient temperature test results and design standards.

Table 7.5 Power-on (POR) / power-off (PDR) reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power-on threshold	T=-40°C to 105°C	1.12	1.50	1.92	V
V_{PDR}	Power-down threshold	T=-40°C to 105°C	0.91	1.24	1.64	V
V_{HSY}	hysteresis	T=-40°C to 105°C	0.122	0.263	0.438	V
t_{RST}	Reset timing	T=-40°C to 105°C	-	3.92	-	ms

Table 7.6 Brown-out reset (BOR) characteristics

Delay selection	Threshold selection	Power-down threshold	Recovery threshold	Hysteresis(mV)	Delay stall(μs)
BOR0	0	1.902	2.015	113	59.96
	1	1.997	2.103	106	63.83
	2	2.205	2.311	106	72.26
	3	2.496	2.612	116	83.82
	4/5/6/7	2.796	2.907	111	95.3

BOR1	0	1.899	2.015	116	120.1
	1	1.994	2.103	109	128.4
	2	2.201	2.311	110	146.4
	3	2.491	2.612	121	171
	4/5/6/7	2.791	2.907	116	195.3

7.7 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 7.7 ESD absolute maximum ratings

Symbol	Parameter	Conditions	Category	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25°C，coincidence ANSI/ESDA/JEDEC JS-001	3B	8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=25°C，coincidence ANSI/ESDA/JEDEC JS-002	C2a	750	V

Table 7.8 Static latch-up/Electrical sensitivity

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25°C	-	±200	-	mA
	V_{supply} over voltage		-	8.25	-	V

7.8 External clock source characteristics

The characteristic parameters given in the following table are measured using a high-speed external clock source

Table 7.9 High-speed external user clock characteristics (HSE)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	User external clock source frequency	-	4	-	20	MHz

C_{HSE}	Recommended load capacitance on OSCIN pin and OSCOUT pin	-	-	-	12(16MHz)	pF
		-	-	-	20(8MHz)	
R_{FHSE}	Feedback resistance	-	-	1	-	MΩ
D_{HSE}	HSE duty factor	-	45	50	55	%
I_{DDHSE}	HSE current consumption	V_{DD}=3.3V, T_A=27℃	-	500	-	uA
t_{SUHSE}	Setup time	-	-	3	-	ms

The characteristic parameters given in the table following were measured using a slow external clock source

Table 7.10 Low-speed external user clock characteristics (LSE)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	User external clock source frequency	-	-	32.768K	-	Hz
C_{LSE}	Recommended load capacitance on OSCIN pin and OSCOUT pin	-	-	12.5	-	pF
R_{FLSE}	Feedback resistance	-	-	5	10	MΩ
D_{LSE}	LSE duty cycle	-	-	50	-	%
I_{DDLSE}	LSE current consumption	SEL=010101 V_{DD}=3.3V, T_A=25℃	-	1.6	-	uA
t_{SULSE}	Setup time	-	-	200	-	ms

7.9 Internal clock source characteristics

The characteristic parameters given in the following table are the data obtained by design simulation and comprehensive test.

High speed internal (HSI) RC oscillator

Table 7.11 High-speed internal (HSI) oscillator characteristics

Symbol	Parameter Conditions	Min	Typ	Max	Unit
V_{DD}	working voltage	2.5	5	5.5	V
f_{HSI}	Frequency VDD=3.3V,TA=27℃	0.994	-	1.006	Mhz
$\Delta temp_{HSI}$	temperature drift(-40~125℃) opposite 27℃,2..5V≤VDD≤5.5V	-1.8	-	1.3	%

ΔVDD_{HSI}	Pressure drift(2.5~5.5V) opposite 3.3V -40~125℃	-0.6	-	0.08	%
$I_{DD(HSI)}$	HSI Oscillator power consumption(1)	-	93.5	-	uA

1.Guaranteed by the design, not tested in production.

Low speed internal (LSI) RC oscillator

Table 7.12 Low-speed internal (LSI) oscillator characteristics

Symbol	Parameter Conditions	Min	Typ	Max	Unit
V_{DD}	working voltage	2.5	5	5.5	V
f_{LSI}	Frequency VDD=3.3V,TA=27℃	32	-	34	Khz
$\Delta temp_{LSI}$	temperature drift(-40~125℃) opposite 27℃,2.5V≤VDD≤5.5V	-0.9	-	2.0	%
ΔVDD_{LSI}	Pressure drift(2~5.5V) opposite 3.3V -40~125℃	-0.7	-	0.8	%
$I_{DD(HSI)}$	HSI Oscillator power consumption	-	1.83(1)	-	uA

1.$I_{DD(LSI)}$ is 1.21μA when VDD is 3.3V

7.10 PLL Characteristics

The characteristic parameters given in the following table are the data obtained by design simulation and comprehensive test.

Table 7.13 PLL Phase-locked loop characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	working voltage	2.5	5	5.5	V
Temp	temperature	-4.0	25	125	℃
f_{PLL_IN}	input clock	-	1	-	Mhz
F_{PLL_OUT}	PLL frequency doubling output clock	-	72	-	Mhz
t_{SU}(PLL)	PLL startup time	51.17	66.2	118.2	μs
I_{DD}(PLL)	PLL power consumption	158.7	315.3	402.1	μA
Jitter	Jitter(peak-to-peak value)	6.609	30.3	53.66	ps

7.11 FLASH memory characteristics

The characteristic parameters given in the following table are guaranteed by design and

are not tested in production.

Table 7.14 FLASH memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A=-40℃~105℃	100			keycles
t_{RET}	Data retention time	T_A=25℃	20	-	-	years
		T_A=105℃	10	-	-	years
t_{PROG}	Byte program time	T_A=-40℃~85℃	43.55	45.75	-	us
t_{ERASE}	Page erase time	T_A=-40℃~85℃ Repeat page erase	1	1.25	-	ms
		T_A=-40℃~85℃ Single pulse page erase mode	4	4.5	-	
t_{MERASE}	Block erase time	T_A=-40℃~85℃	8	10	-	ms

7.12 ADC characteristics

Unless otherwise specified, the parameters in the following table are measured using the required ambient temperature, clock frequency, and VDDA supply voltage.

Table 7.15 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	working voltage	-	2.5	3.3	5.5	V
V_{IN}	ADC input voltage	Single-ended input mode	V_{SSA}	-	V_{DDA}	V
$I_{DD(ADC)}$	ADC operating current	V_{DDA}=3.3V,TA=25℃ , bias current 15uA	-	2.9	-	mA
I_{ADCIN}	ADC input current	V_{DDA}=3.3V,TA=25℃	-	-	1	uA
f_{ADC}	ADC clock frequency	-	1.5	24	30	Mhz
f_s	ADC Sampling conversion rate	V_{DDA}=3.3V,TA=25℃ bias current 15uA	-	-	1	MSPS
t_s	ADC Sampling time	-	3	-	1024	$1/f_{ADC}$
t_{CONV}	ADC total conversion time (sampling + interval + conversion)	Resolution 12 bits	21~1024			$1/f_{ADC}$
R_s	ADC input switch equivalent resistance	RC filtering	-	1.2	-	K Ω
		No RC filtering	-	2.3	-	
ADC_{RESO}	resolution	-	12			Bit
ENOB	Actual effective number of bits	V_{DDA}=3.3V,TA=25℃	9.5	10	-	Bit
DNL	Differential nonlinearity	2.5V≤V_{DDA}≤5.5V, TA=25℃	-	-	±1.5	LSB
INL	Nonlinearity of integral		-	-	±2	LSB
EO	Misalignment error		-	-	±2.5	LSB
EG	Gain error		-	-	±2	LSB
EF	Full scale error		-	-	±4	LSB
SNDR	signal-to-noise distortion ratio	2.5V≤V_{DDA}≤5.5V, 40Khz-0.02dBFS	66	-	-	dB
THD	All harmonic distortion		-	-	-72	dB

1. In addition to special instructions, the typical value is the measured value at 25℃ .

Power consumption of ADC under different bias current configurations

The microcontroller is under the following conditions :

TA = 25℃. The channel pin is connected to a 10K sliding rheostat, and the input voltage of the ADC channel is kept at 2.5V. The current consumption of the MCU under the continuous sampling condition of the ADC is measured by changing the bias current.

ADC configuration status : 12 bit resolution, sampling comparison interval is 0, sampling

conversion interval is 0, sampling time configuration is the largest.The current consumption test results are shown in the following table.

Table 7.16 ADC bias current and current consumption

working voltage	bias current	power consumption (mA）	working voltage	bias current	power consumption(mA）
3.3V	OPAMP_5UA + COMP_12UA	3.84	5V	OPAMP_5UA + COMP_12UA	3.7
	OPAMP_5UA + COMP_10UA	3.3		OPAMP_5UA + COMP_10UA	3.13
	OPAMP_5UA + COMP_9UA	3.08		OPAMP_5UA + COMP_9UA	2.9
	OPAMP_5UA + COMP_7UA	2.68		OPAMP_5UA + COMP_7UA	2.41
	OPAMP_5UA + COMP_5UA	2.2		OPAMP_5UA + COMP_5UA	1.85
	OPAMP_5UA + COMP_4UA	1.96		OPAMP_5UA + COMP_4UA	1.61
	OPAMP_5UA + COMP_2UA	1.46		OPAMP_5UA + COMP_2UA	1.05
	OPAMP_4UA + COMP_12UA	3.74		OPAMP_4UA + COMP_12UA	3.67
	OPAMP_4UA + COMP_10UA	3.29		OPAMP_4UA + COMP_10UA	3.13
	OPAMP_4UA + COMP_9UA	3.07		OPAMP_4UA + COMP_9UA	2.88
	OPAMP_4UA + COMP_7UA	2.59		OPAMP_4UA + COMP_7UA	2.33
	OPAMP_4UA + COMP_5UA	2.1		OPAMP_4UA + COMP_5UA	1.77
	OPAMP_4UA + COMP_4UA	1.86		OPAMP_4UA + COMP_4UA	1.51
	OPAMP_4UA + COMP_2UA	1.37		OPAMP_4UA + COMP_2UA	0.95
	OPAMP_3UA + COMP_12UA	3.65		OPAMP_3UA + COMP_12UA	3.6
	OPAMP_3UA + COMP_10UA	3.19		OPAMP_3UA + COMP_10UA	3.06
	OPAMP_3UA + COMP_9UA	2.98		OPAMP_3UA +	2.82

OPAMP_3UA + COMP_7UA	2.51
OPAMP_3UA + COMP_5UA	2.02
OPAMP_3UA + COMP_4UA	1.79
OPAMP_3UA + COMP_2UA	1.28
OPAMP_2UA + COMP_12UA	3.56
OPAMP_2UA + COMP_10UA	3.12
OPAMP_2UA + COMP_9UA	2.89
OPAMP_2UA + COMP_7UA	2.42
OPAMP_2UA + COMP_5UA	1.92
OPAMP_2UA + COMP_4UA	1.69
OPAMP_2UA + COMP_2UA	1.25

COMP_9UA	
OPAMP_3UA + COMP_7UA	2.26
OPAMP_3UA + COMP_5UA	1.7
OPAMP_3UA + COMP_4UA	1.44
OPAMP_3UA + COMP_2UA	0.88
OPAMP_2UA + COMP_12UA	3.5
OPAMP_2UA + COMP_10UA	2.97
OPAMP_2UA + COMP_9UA	2.72
OPAMP_2UA + COMP_7UA	2.15
OPAMP_2UA + COMP_5UA	1.6
OPAMP_2UA + COMP_4UA	1.34
OPAMP_2UA + COMP_2UA	0.78

7.13 Standard SPI characteristics

Table 7.17 Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Master	-	-	16M	Hz
		Slave	-	-	8M	
$t_{SCK(H)}$	SCK high time	...	31	-	-	ns
$t_{SCK(L)}$	SCK low time	...	31	-	60	ns
$t_{V(MO)}$	Master data output valid time	...	-	-	-	ns
$t_{H(MO)}$	Master data output hold time	...	2	-	-	ns
$t_{SU(MI)}$	Master input setup time	...	5	-	-	ns
$t_{H(MI)}$	Master input hold time	...	5	-	-	ns
$t_{SU(NSS)}$	NSS enable setup time	...	125	-	-	ns
$t_{H(NSS)}$	NSS enable hold time	...	62	-	-	ns

$t_{A(SO)}$	Slave data output arrive time	...	-	-	38	ns
$t_{DIS(SO)}$	Slave data output disappear time	...	3	-	10	ns
$t_{V(SO)}$	Slave data output valid time	...	-	-	120	ns
$t_{H(SO)}$	Slave data output hold time	...	15	-	-	ns
$t_{SU(SI)}$	Slave data input setup time	...	5	-	-	ns
$t_{H(SI)}$	Slave data input hold time	...	4	-	-	ns

7.14 IIC characteristics

Table 7.18 IIC characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Super fast mode		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	...	0	100	0	400	-	1M	Hz
$t_{SCL(H)}$	SCL clock high time	...	4.0	-	0.6	-	0.3	-	us
$t_{SCL(L)}$	SCL clock low time	...	4.7	-	1.3	-	0.7	-	us

7.15 Internal reference voltage characteristics

The characteristic parameters given in the following table are the data obtained through design simulation and comprehensive test.

Table 7.19 Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{REFINT}	Internal reference voltage	-40℃<TA < 105℃ , 2.5V≤V_{DDA}≤5.5V	1.186	1.214	1.241	V
$T_{S\_VREFINT}$(1)	ADC sampling time when reading internal reference voltage	-	3	-	-	us
ΔV_{REFINT}(1)	Internal reference voltage distribution over the entire temperature range	-40℃<TA < 105℃, V_{DDA} =3V	1.184	1.213	1.228	mV
T_{coeff}(1)	Temperature coefficient	-	22.88	23.36	61.77	ppm/℃
T_{start}(1)	Startup time	-	47.99	65.99	82.41	us

1. Guaranteed by design, not tested in production.

Table7.20 Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Adjust the internal reference voltage after calibration T_A=25℃ ， V_{DDA}=3.3V	0x0002 0300

7.16 Internal temperature sensor characteristics

The characteristic parameters given in the following table are the data obtained through design simulation and comprehensive test.

Table7.21 Inter temperature sensor characteristics

Symbol	Parameter	Min	Typical	Max	Unit
Avg_Slope(1)	Average slope	3.12	3.206	3.237	mV/℃
V_{25}	Voltage at 25℃	951.2	964.4	976.1	mV
V_{27}	Voltage at 27℃	957.5	970.8	982.6	mV
T_{START}(1)	Start Time	3.876	7.709	12.97	us
T_{S_TEMP}(1)	ADC sampling time when reading internal temperature	3	-	-	us

1. Guaranteed by design, not tested in productio

8 Package Information

BYD Semiconductor provides a variety of packaging forms according to different environments to meet the needs of different scenarios. At present, the first generation has LQFP64 and LQFP48 packaging. Consult the packaging manufacturer for specific packaging information.

8.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 8.1 LQFP48 package outline

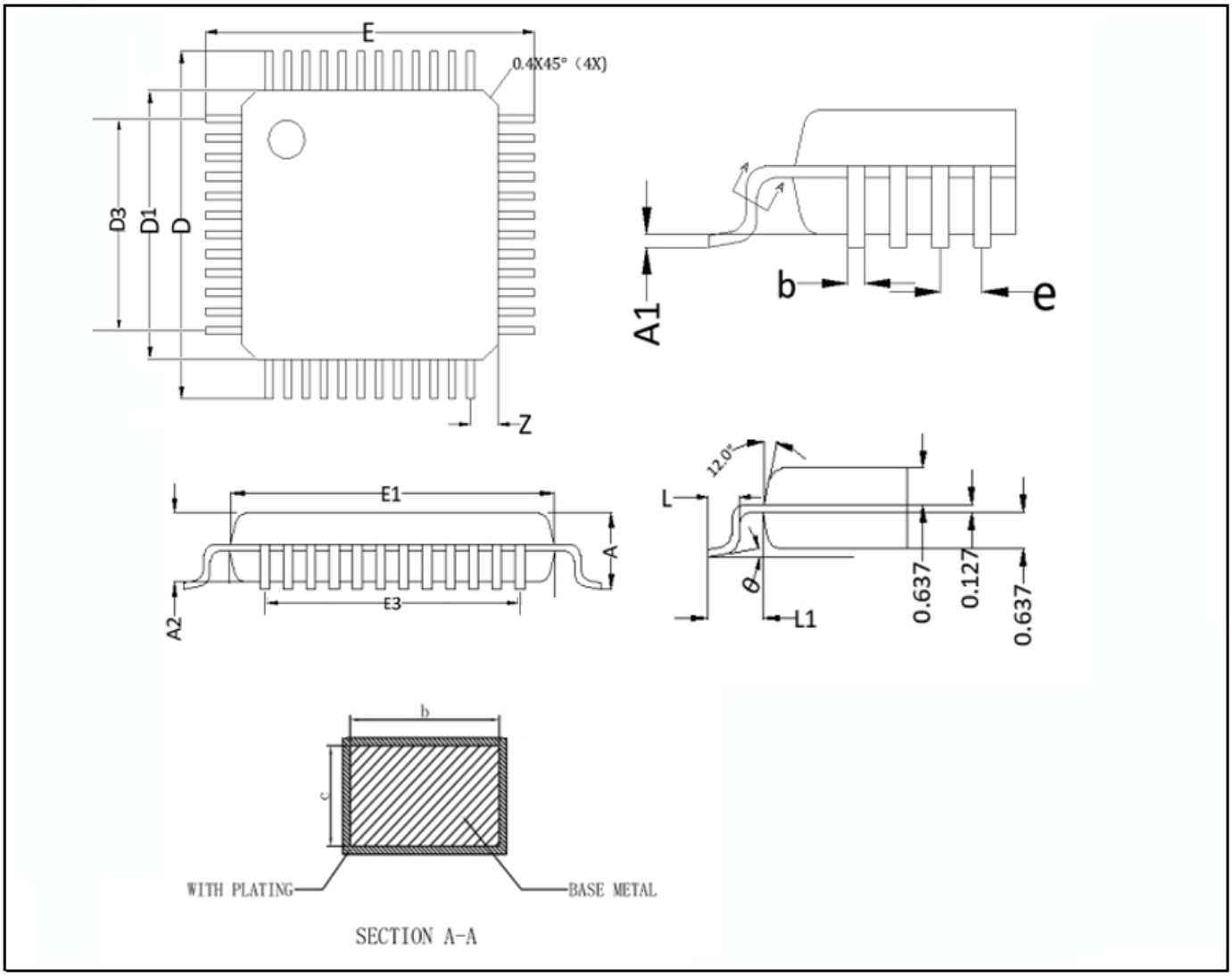


Table 8.1 LQFP48 mechanical data

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.035	-	0.079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3	-	5.50	-	-	0.2165	-
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
θ	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.003

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8.2 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 8.2 LQFP64 package outline

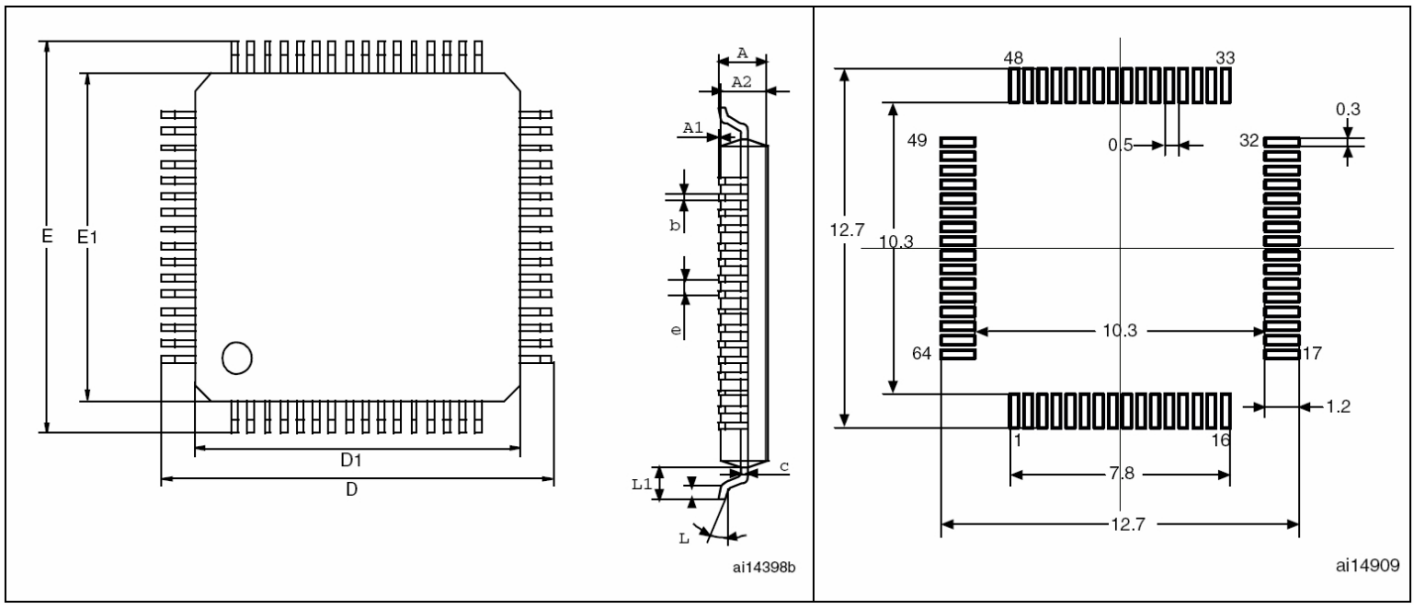


Table 8.2 LQFP64 mechanical data

Symbol	millimeters			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8.3 Attentioan

1. **Chip validity: 1 year under vacuum sealed package**
2. **Baking requirements: the products must be baked at high temperature (125℃ bake 8H) before going on SMT, and the unused products must be baked at high temperature (125℃ bake 8H) before going online.**
3. **Storage environment: constant temperature and humidity 20±5℃ humidity 30%-60%(vacuum sealed package)**
4. **Humidity sensitivity level: MSL3 requires that it should be used online within 168 hours after unpacking**

9 Packing Information

9.1 Tray

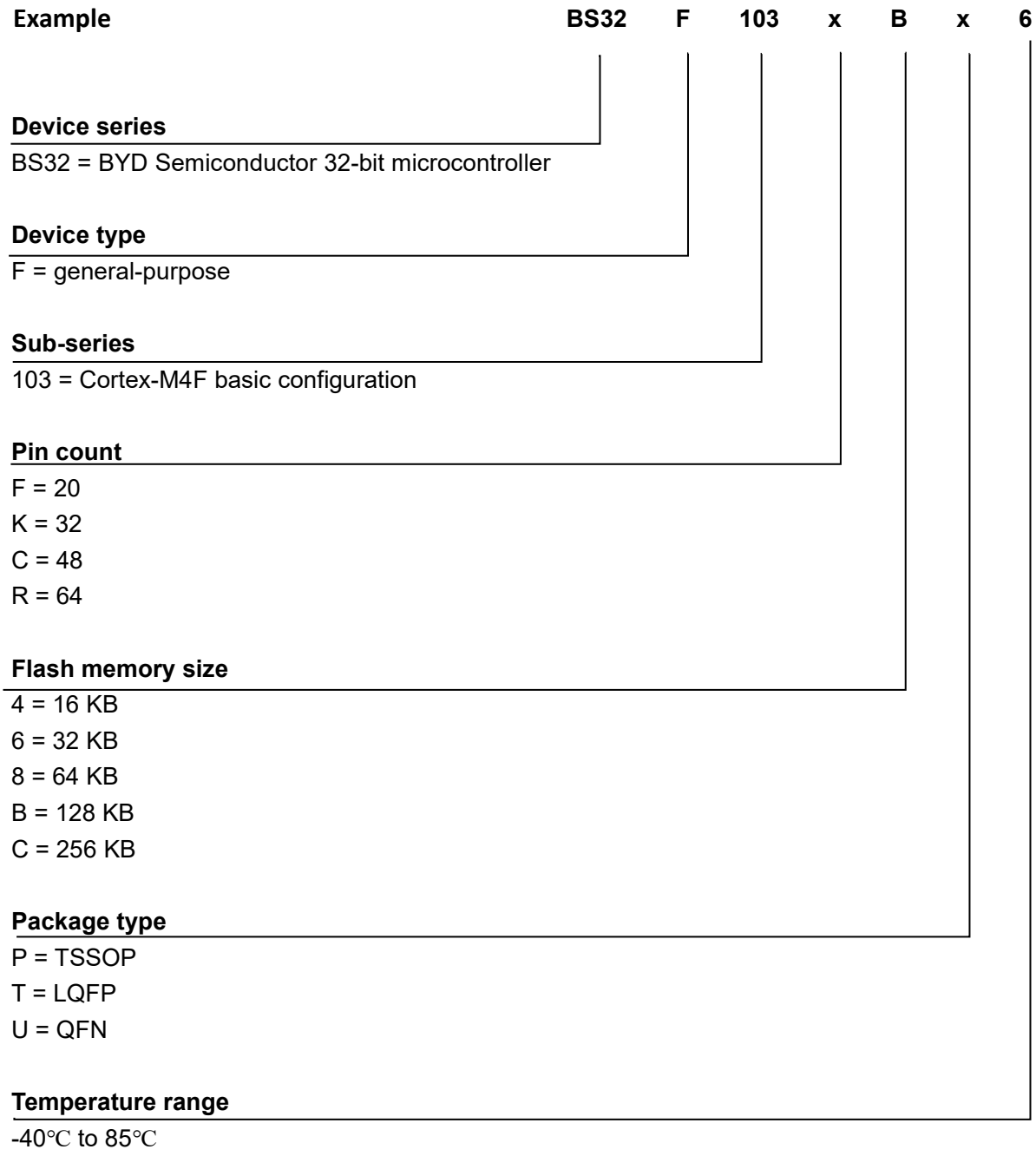
With desiccant,humidity indicator card,put into an anti_static bag,and vacuum

9.2 Packing quantity

Table 9.1 package information

Package form	Piece/Plate	Plate/pack	Piece/pack	Pack/Box	Piece/Box	Packaging method
LQFP48	250	10	2500	6	15000	Tray
LQFP64	160	10	1600	6	9600	Tray

10 Ordering Information



11 Revision History

Tbale 10.1 Document revision history

Version	Data	Description
V1.0.0	22/12/2022	Initial release
V1.0.1	24/03/2023	Updated electrical characteristics content

12 Glossary

Table 11.1 gives a brief definition of acronyms and abbreviations used in this document:

Table 12.1 Terminology List

Terminology	Definition
ADC	Analog-digital converter
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
CRC	Cyclic redundancy check calculation unit
DMA	Direct memory access
ESD	Electro-Static discharge
EXTI	Extended interrupt/event controller
FLASH	Flash memory
GPIO	General-purpose input/output
HSE	High-speed external clock
HSI	High speed internal clock
I2C	Inter-integrated circuit interface
IWDG	Independent watchdog
LSE	Low-speed external clock
LSI	Low-speed internal clock
NVIC	Nested vectored interrupt controller
PDR	Power-down reset
PLL	Phase locked loop
POR	Power-on reset
RAM	Random access memory
RTC	Real-time clock
SPI	Serial peripheral interface
SRAM	Static random access memory
SW-DP	Serial wire debug port
TAMP	Tamper and backup
TIM	Timer
TS	Temperature sensor
UART	Universal asynchronous receiver/transmitter
WWDG	Window watchdog

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